R18 Regulation Subject code: 2P4EB

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A' Grade)

B.Tech IV Semester Supplementary Examinations, September 2023

Computer Organization

(CSE)

Maximum Marks: 70 Date:15.09.2023 Duration: 3 hours

Note: 1. This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10x2M=20 Marks)

1 What is an interrupt cycle?
2 Define the control memory and control word.
3 Explain the 8086 instruction format.
4 Write down the functions performed by BIU and EU
5 Explain Instruction pipelining.
6 Explain Fixed point representation.
7 Explain about connection of I/O bus to input output devices.
8 What is the concept of polling.
9 What is an inter process arbitration
10 What is a crossbar switch

Part-B

Answer All the following questions. (5X10M=50Marks)

11 What is the difference between a direct and indirect address instruction. Explain about instruction cycle with a neat sketch. (10M)

OR

12 What is an instruction cycle and write the flowchart for instruction cycle. (10M)

13 Discuss the concept of segmented memory.what are its disadvantages. (10M)

OR

14 a) Explain about register organization in 8086 (5M)
b) Explain about the concept of segmented memory with a neat diagram. Explain it's advantages. (5M)

15 What is handshaking? Explain source-initiated and destination initiated data transfer using handshaking (10M)

OR

16 a) What is asynchronous data transfer? Explain in detail. (5M)
b) How can you justify Daisy Chain priority is useful in priority interrupt? (5M)

17 What is mapping process? What are the different types of mapping procedures (10M)

OR

18 Explain about the cache memory and its advantages. (10M)

19 Explain about the time shared common bus and discuss the structure for multiprocessors (10M)

OR

20 Define RISC and explain the concept of delayed load and delayed branch (10M)