Regulation R17 *Subject code: 1P4BA*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A' Grade)

B.Tech II Year II Semester Supplementary Examinations, September 2023

SWITCHING THEORY AND LOGIC DESIGN

(EEE)

Maximum Marks: 70 Date:13.09.2023 Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10x2M=20 Marks)

1 Write about positional weighted codes and non-positional weighted codes with an example.

2 Find the 2's complement of
i).11101010 ii) 01111110

3 What is the use of the K-map.

4 Write short notes on parity encoder.

5 Define a combinational circuit with block diagram.

6 Difference between a latch and a flip-flop.

7 Define the ripple counter,

8 What is the SISO.

9 Define i) state table ii) state diagram.

10 Write Hazards types in sequential circuits.

Part-B

Answer All the following questions. (5X10M=50Marks)

11 a) Implement AND, OR, NOR by using NAND gates only. [5]
b) Derive the Hamming code for the sequence (101011) [5]

OR

12 Simplify the following Boolean expressions using the Boolean theorems. (i) (A+B+C) (B'+C) + (A+D) (A'+C) (ii) (A+B) (A+B') (A'+B) [10]

13 Obtain the simplified expression in POS (product of sums) of $F(w,x,y,z)=\pi(1,2,4,7,12,14,15)$ using K-maps [10]

OR

14 a)Define a multiplexer? Draw 2:1 multiplexer for the function $f(x,y,z)=\sum(0,2,3,5,7)$ [4]
b)Design a 4-bit binary to gray code converter and draw the AOI logic circuit [6]

15 What is the drawback of JK flip flop, Design a flip flop which overcomes this drawback and explain with neat diagram. [10]

OR

16 a) Convert SR flip flop to JK flip flop [5]

b) What is the difference between D-latch and D-flip flop and draw the timing diagram for both. [5]

17 a) Explain about serial in parallel out shift register with a neat diagram. [5]

b) Design a synchronous counter with T-flip flops that goes through the binary repeated sequence 0,1,3,7,6,4,0,1….. [5]

OR

18 a) Design a Twisted ring counter with state table and state diagram [7]

b) Difference between RAM and ROM [3]

19 Explain about Mealy and Moore machines with neat diagrams. [10]

OR

20 a) Write the steps in analyzing of sequential circuit? [5]

b) Write capabilities and limitations of finite state machines? [5]