R18 Regulation *Subject code:* 2E8DE

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A' Grade)

B.Tech VIII Semester Regular Examinations, June 2022

DESIGN OF FAULT TOLERANT SYSTEMS

(ELECTRONICS AND COMMUNICATION ENGINEERING)

Maximum Marks: 70 Date:18.06.2022 Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10x2M=20 Marks)

1 What is meant by MTBF?
2 Distinguish between failures and faults.
3 List the advantage of self-checking circuits.
4 What is meant by fail safe design?
5 Give the significance of testability.
6 What are shadow registers? Mention their purpose.
7 Name some types of BIST.
8 What is meant by Test pattern generator?
9 What is the purpose of boundary scan test?
10 Define TAP controller.

Part-B

Answer All the following questions. (5X10M=50Marks)

11 Explain in detail about Time redundancy and Software redundancy schemes. [10]

OR

12 A) Define Reliability and Failure rate and derive the relationship between these two parameters. [5]
B) Discuss about the reliability of series-parallel and parallel- series systems. [5]

13 Explain Berger code for a totally self checking checker. Information bits I= 0101000, calculate check bits and Berger code. Design a totally self-checking checker for the information bits. [10]

OR

14 A) Discuss about the fail safe design of sequential circuits using partition theory. [5]
B) Discuss about totally self-checking PLA design. [5]

15 A) With a neat diagram, explain the Reed-Muller's expansion technique for $f=WX+WY+XY$. [7]
B) What are the draw backs of Reed-Muller expansion Technique. [3]

OR

16 A) Explain the multiple scan design. [5]
B) Explain controllability and observability by means of scan register. [5]

17 Explain the basic architecture of BIST and the different types of BIST. [10]

OR

18 A) Discuss importance of BIST for VLSI chips. [3]
B) Discuss various test pattern generations for BIST exhaustive testing with example. [7]

19 Explain the Board level scan chain structure. [10]

OR

20 Discuss the following: i) RT level boundary scan ii) boundary scan description language [5]+ [5]