Regulation R18 *Subject code: 2P4DD*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A' Grade)

B.Tech V Semester Supplementary Examinations, July 2022
LINEAR & DIGITAL IC APPLICATIONS
(ECE)

Maximum Marks: 70 Date:04.07.2022 Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks **(10x2M=20 Marks)**

1 Write down the applications of Operational amplifier.
2 Define CMRR.
3 Define lock range and capture range in a PLL.
4 Draw the Low pass filter frequency response.
5 Define quantization error in an ADC.
6 Mention the advantages of R-2R ladder DAC.
7 Define noise margin and propagation delay.
8 Write down the need of parity generator/checker IC.
9 What is race around condition? How is it avoided?
10 Write the functions of Universal shifter?

Part-B

Answer All the following questions. **(10M X 5=50Marks)**

11. Explain ideal characteristics of an op-amp. 10

OR

12. Write down the need of voltage regulator. Explain IC 723. 10

13 Explain triangular waveform generator using IC 741 and derive frequency of oscillations. 10

OR

14. Draw the block diagram of 565 PLL and explain about each block. 10

15. Explain the R-2R ladder DAC with neat diagram. 10

OR

16. Explain the working of a parallel comparator type A/D converter. 10

17 Design BCD to gray code converter. 10

OR

18 Explain with neat diagram interfacing of TTL gate driving CMOS and CMOS driving TTL Gates.

19 Design a 3- bit synchronous counter.

OR

20. Design a Modulo-12 ripple counter using IC 74×74.