Regulation R17 *Subject code:1E5DE*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A' Grade)

B.Tech III Year I Semester Supplementary Examinations, July 2022
Digital Design Through Verilog HDL

(ECE)

Maximum Marks: 70 ***Date:07.07.2022*** Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks **(10x2M=20 Marks)**

1	Explain simulation and synthesis with differences	02
2	Mention data types used in Verilog HDL	02
3	Illustrate with an example Array of Instances of Primitives	02
4	Define net delay with an example	02
5	Write about Bitwise operators in Verilog	02
6	Write about bidirectional gates	02
7	Write the syntax of event construct	02
8	Write a Verilog module for 2 to 4 decoder using case statement	02
9	Write about $display task	02
10	Write a simple UDP table for 2 input AND gate	02

Part-B

Answer All the following questions. **(10M X 5=50Marks)**

11	a) Explain levels of design description	06
	b)Differentiate between vectors and memories	04
	OR	
12	a) Explain the following "lexical conventions" with examples (i) key words (ii) identifiers (iii) Numbers	06
	b)Explain about data types in Verilog	04
13	a) Design full adder using basic logic primitives	05
	b) Write the Verilog code for 4 X1 Multiplexer using the tri-state buffer in the gate level modeling.	05
	OR	
14	a)Explain about strengths and strength contention resolution with an example	06

	b)Design 8 to3 encoder in gate level model	04
15	a) Explain about operators in Verilog	05
	b) Design CMOS switch of parallel combination	05
	OR	
16	a)Write a Verilog code for CMOS inverter	05
	b)Design 2 input NAND gate in switch level modeling	05
17	a)Explain case construct with an example	05
	b) Differentiate between blocking and non-blocking statements in behavioral model	05
	OR	
18	a) Design 4:1 multiplexer using if else construct	05
	b) Explain clocked JK flip flop Verilog module and test bench	05
19	a)Briefly explain combinational UDPs in Verilog	05
	b) Differentiate between tasks and Functions	05
	OR	
20	Explain about sequential UDPs with an example	10