R20 Regulation *Subject code:* 3P4FB

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A' Grade)

B.Tech IV Semester Regular Examinations, July 2022

COMPUTER ORGANIZATION

(Information Technology)

Maximum Marks: 70 Date: 22.07.2022 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10x2M=20 Marks)

1 Explain the basic components of Generic Computing system
2 Differentiate High level and Low-level languages.
3 Draw the general configuration of Micro programmed Control unit.
4 Write about the operation on Memory-Mapped I/O.
5 List out the general aspects of ROM, RAM and IO interfacing modules.
6 How Virtual address Mapping using Pages to solve the fetching process?
7 Tabulate the Input-Output Instructions using register transfer notations.
8 Write about Auxiliary memory devices.
9 Write the steps involved in Branching operation.
10 List some of sorting mechanisms.

Part-B

Answer All the following questions. (10MX 5=50Marks)

11 With suitable paradigms, describe the Instruction Formats with One address, two addresses, zero addresses and three addresses. [10]

OR

12 What is an Interrupt? Draw block diagram for a bidirectional input/output device with its interface. [10]

13 Explain the appropriate method to solve the problem faced in Asynchronous Input / Output Synchronization. [10]

OR

14 Elaborate how DMA bypasses CPU and speeds up the memory operation? With a neat schematic, Explain about DMA controller and its mode of data transfer. [10]

15 What is virtual memory? Explain the relation between address space and memory space in a virtual memory system along with its memory table for mapping. [10]

OR

16 What is Locality of Reference and explain about Cache memory in detail? Illustrate the mapping process involved in transformation of data from main to Cache memory. [10]

17 Draw and explain the schematic of 8086 architecture with a neat block diagram. [10]

OR

18 Illustrate the basic addressing modes of 8086 architecture with the use of Memory and Register. [10]

19 Elaborate the register transfer mechanism for Branch & Call instructions. [10]

OR

20 Write an Assembly Language Programs involving evaluation of Arithmetic Expressions. [10]