



R20 Regulation
TKR COLLEGE OF ENGINEERING AND TECHNOLOGY
(Autonomous, Accredited by NAAC with 'A' Grade)

Subject code: 3P4BB

B.Tech IV Semester Regular Examinations, July 2022
Digital Electronics
(Electrical and Electronics Engineering)

Maximum Marks: 70

Date: 22.07.2022 Duration: 3 hours

- Note: 1. This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks

(10x2M=20 Marks)

- 1 Convert the binary number 101101 into gray code
- 2 Convert 56_{10} to its equivalent a) binary, b) hexadecimal
- 3 State DeMorgan's Theorem.
- 4 Why NAND and NOR gates are called as universal gates?
- 5 What is multiplexer? Mention its applications.
- 6 Draw the logic diagram of half subtractor.
- 7 Differentiate Combinational and Sequential Circuits
- 8 Write a brief note on triggering.
- 9 Define Merger Chart.
- 10 Compare Mealy and Moore Model.

Part-B

Answer All the following questions.

(10MX 5=50Marks)

- 11 If the 7 bit hamming code word received by the receiver is 1011011 assuming the even parity state whether the received code word is correct or wrong. If so, locate the bit having error and write the corrected code.

OR

- 12 A. Fill the table by doing conversion (6)

Decimal	Binary	Octal	Hexa-decimal
33			
	1110101		

- B. Determine twos complement of 110011. (2)
C. Write the binary and BCD code for decimal number 44. (2)
- 13 Simplify using tabulation method
 $F = \sum(0,5,7,8,9,10,11,14,15)$

OR

- 14 Simplify using K-map and implement using logic gates $B'D+A'BC'+AB'C+ABC'$
- 15 Implement the full adder circuit using decoder and explain.

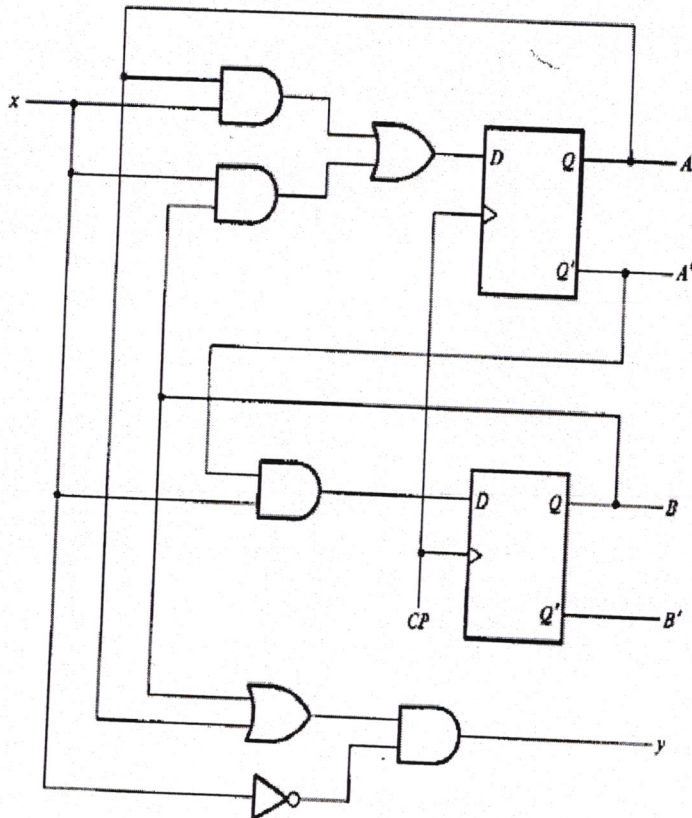
OR

- 16 A. What are hazards? How it can be avoided? (4)
B. Design a hazard free circuit for the following Boolean function. (6)
 $F = \sum(0,2,6,7,8,10,12)$

- 17 Design a SR flipflop using NAND gates and write its characteristic equation, characteristic table and excitation table.

OR

- 18 Design a BCD ripple counter using JK flipflop.
- 19 For the logic diagram shown below,
(A) Obtain the expression (i) input equation (2)
(ii) state equation (2)
(iii) output equation (1)
(B) Write the state table. (3)
(C) Draw the state diagram. (2)



OR

20 A sequential circuit with two D flipflops A and B, two inputs, x and y, and one output z is specified by the following next-state equations and output equations.

$$A(t+1) = x'y + xA$$

$$B(t+1) = x'B + xA$$

$$Z=B$$

- (i) Draw the logic diagram of the circuit (4)
- (ii) List the state table for the sequential circuit. (4)
- (iii) Draw the corresponding state diagram. (2).