

Regulation R18

Subject code: 2P4DD



TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A' Grade)

B.Tech IV Semester Supplementary Examinations, July 2022

LINEAR & DIGITAL IC APPLICATIONS

(Electronics and Communication Engineering)

Maximum Marks: 70

Date:28.07.2022 Duration: 3 Hours

Part-A

All the following questions carry equal marks

(10x2M=20 Marks)

- 1 Define unity gain bandwidth of an op-amp.
- 2 What is slew rate?
- 3 Define VCO.
- 4 List the applications of 565 PLL.
- 5 What do you mean by quantization error in an ADC?
- 6 List the broad classification of ADCs.
- 7 What is a mean by a combinational circuit?
- 8 Define Propagation delay.
- 9 List the basic types of shift registers interns of data movement.
- 10 Define Dynamic RAM.

Part-B

Answer all the question.

(10MX 5=50Marks)

- 11 Explain AC & DC characteristics of an operational amplifier. 10M  
OR
- 12 a) Design a differentiator circuit that will differentiate input signal with  $f_{max} = 100\text{Hz}$ . 5M  
b) What is a comparator? Discuss the Non inverting comparator and obtain output waveforms for various inputs. 5M
- 13 Draw the circuit diagram of RC phase shift oscillator and derive the expression for its frequency of oscillations.10M  
OR
- 14 Draw the block diagram of an Astable multivibrator using 555timer and derive an expression for its frequency of oscillations. 10M
- 15 Give the schematic circuit of integrating type A/D converter and explain the operation of this system and derive expression for output voltage  $V_o$ . 10M  
OR
- 16 a) Draw the circuit diagram of R-2R ladder DAC and explain its operation. 5M  
b) Write the disadvantages of R-2R Ladder DAC. 5M
- 17 a) Explain the operation of 74LS148 encoder. 5M  
b) Realize the following expression using 74X151 IC  $F(Y) = AB+BC+AC$ . 5M  
OR
- 18 Sketch and explain the operation of CMOS transmission gate. 10M
- 19 a) Discuss how PROM, EPROM and EEPROM technologies differ. 5M  
b) Compare PROM, PLA and PAL. 5M  
OR
- 20 Explain the functional behavior of Static RAM cell? Show the internal structure of  $8 \times 4$  static RAM. 10M