Regulation R17 *Subject code: 1P4BA & 1P4DA*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A' Grade)

B.Tech II Year II Semester Supplementary Examinations, July 2022

SWITCHING THEORY AND LOGIC DESIGN

(Common to EEE & ECE)

Maximum Marks: 70 Date:20.07.2022 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10x2M=20 Marks)

1	What are the different illegal states of BCD and XS-3?	[2]
2	What is self-complementing code? Give example.	[2]
3	Write truth table of NAND gate.	[2]
4	What is a decoder? Write its applications.	[2]
5	Define Level trigger, Edge trigger.	[2]
6	Define Combinational logic circuit.	[2]
7	What are registers? Write any two applications.	[2]
8	What are the drawbacks of ripple counters?	[2]
9	Define merger graph of n-state machine M.	[2]
10	Write Application of sequence detector	[2]

Part-B

Answer All the following questions. (10M X 5=50Marks)

11	a) Convert the gray number 101101 into: i) Decimal ii) Octal iii) Hex	[5]
	b) Perform the subtraction in BCD using 9's complement method for 592.6-887.9.	[5]
	OR	
12	a) Derive the Boolean expression for a two input Ex-OR gate to realize with the two input NAND gates without using complemented variables and draw the circuit.	[5]
	b) Expand (A+D')(A+C')(A'+B)(A'+B+C) into max terms and min terms.	[5]
13	Minimize the following expression using K-map and realize using NAND Gates. $F(A,B,C,D) = \sum m(0,1,2,9,11) + d(8,10,14,15)$.	[10]
	OR	
14	Simplify the following Boolean function using Tabular method. $F(A,B,C,D)=\sum m(0,1,2,5,7,8,9,10,13,15)$	[10]

15 Design 8:1 Mux using 2:1 Mux and explain in detail. [10]

OR

16 Draw the circuit diagram of J-K flip flop with NAND gates with positive edge triggering and explain its operation with the help of truth table. How race around condition is eliminated. [10]

17 Design a mod-12 Ripple counter using T flip flops and explain its operation. [10]

OR

18 Draw and explain the operation of the Master Slave SR flip-flops with block diagram. [10]

19 Explain the procedure of Mealy to Moore conversion. [10]

OR

20 a) What are the capabilities and limitations of finite state machines? Discuss. [5]

b) Explain about Merger graph and Merger table [5]