



R20 Regulation

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A' Grade)

B.Tech VI Semester Regular Examinations, June/July 2023

Subject code:3P6DD

VLSI DESIGN

(Electronics and Communication Engineering)

Maximum Marks: 70

Date:30.06.2023 Duration: 3 hours

- Note:
- 1.This question paper contains two parts A and B.
 2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
 3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
 4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks

(10x2M=20 Marks)

- 1 How the MOSFET is used for amplifying electronic signals?
- 2 What is inversion mode in MOS transistor?
- 3 Why nMOS transistor is selected as pull down transistor?
- 4 Define and give the expressions for any four scaling factors of MOS device parameters.
- 5 Explain the formal estimation of CMOS Inverter delay.
- 6 What are the sources of wiring capacitances?
- 7 Design a 2-bit Parity generator.
- 8 Mention about SRAM and its usage.
- 9 What are the characteristics of FPGA?
- 10 What is the need for testing?

Part-B

Answer All the following questions.

(10MX 5=50Marks)

- 11 Draw and explain the fabrication steps of NMOS transistor. (10M)
OR
- 12 Derive the relationship between I_{ds} and V_{ds} . (10M)
- 13 Write the layout design rules and draw the layout diagram for CMOS Inverter gate. (10M)
OR
- 14 What is stick diagram and explain about different symbols used for components in Stick diagram. Draw the stick and layout for a two input CMOS NAND gate. (10M)
- 15 A. What are the issues involved in driving large capacitor loads in VLSI circuit regions? Explain. (7M)
B. Calculate the gate capacitance value of 5mm technology minimum size transistor with gate to channel value is 4×10^{-4} pF/mm². (3M)
OR
- 16 What are different types of alternate gate circuits? Explain any two models. (10M)
- 17 A. Draw the basic block diagram of 4-bit adder and explain its operation in detail. (5M)
B. Give a short note on Zero/One Detectors. (5M)
OR

- 18 A. Draw the basic circuit diagram of static RAM and explain its operation. (5M)
B. Explain about Serial access memories. (5M)
- 19 A. What are the draw backs of PLAs? How PLAs are used to implement combinational and sequential logic circuits? (5M)
B. Discuss the types of FPGA routing techniques. (5M)
- OR
- 20 A. Explain Chip level Test Techniques. (5M)
B. Why stuck-at faults occur in CMOS circuits? Explain with suitable logical diagram. (5M)