R20 Regulation *Subject code: 3E5DA*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A' Grade)

B.Tech V Semester Supplementary Examinations, June/July 2023

DIGITAL DESIGN THROUGH VERILOG HDL

(Electronics and Communication Engineering)

Maximum Marks: 70 Date:06.07.2023 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10x2M=20 Marks)

1 Describe the steps in ASIC design flow?
2 Write about white space character with an example.
3 What is Tri-state Gates?
4 What is array of instances of primitives?
5 Define operators in Verilog.
6 What do we mean by continuous assignment?
7 How can the timing checks be given in system tasks in Verilog?
8 What is the main advantage of the adjustable parallel block?
9 Define path delay.
10 What is the use of define directives?

Part-B

Answer All the following questions. (10MX 5=50Marks)

11 Explain different levels of design description in Verilog. (10M)

OR

12 What are the Tokens available in Verilog HDL? Discuss them with the necessary syntax and an example. (10M)

13 Write a Verilog code for following digital circuit using gate level modeling.
(i) JK flip flop (5M) (ii) 3-8 Decoder (5M)

OR

14 Design a Full adder using Verilog HDL (Gate Level Modeling). (10M)

15 Explain the Types of Operators in Data Flow Modeling with example. (10M)

OR

16 A.Explain the Transistor switch and bi-directional switch. (5M)
B.Write a program for NMOS Three input NOR gate? (5M)

17 Write Verilog code for 1:8 demultiplexer in behavioral model. (10M)

OR

18 A.Write short notes on non-blocking assignments and what are the sequences takes place at each positive edge of the clock for the non-blocking assignments. (5M)
B.Explain behavioural models of the finite state machine. (5M)

19 What are the differences between Tasks and Functions? Explain with an example. (10M)

OR

20 Briefly explain combinational and sequential UDPs in Verilog. (10M)