Regulation R18 *Subject code: 2P5DB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A' Grade)

B.Tech V Semester Supplementary Examinations, June/July 2023

VLSI DESIGN

(Electronics and Communication Engineering)

Maximum Marks: 70 Date:26.06.2023 **Duration: 3 Hours**

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 10 questions. Answer any 5 questions which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions. Each carry equal marks (10x2M=20 Marks)

1 Define g_m of MOS transistor.
2 What are the advantages of BiCMOS over CMOS?
3 Define scaling.
4 Sketch a stick diagram for CMOS inverter.
5 What is switch logic?
6 What is fan-in of a gate?
7 Draw the circuit diagram of SRAM cell.
8 What is parity generator?
9 Implement Half adder using PAL.
10 What are functionality tests?

Part-B

Answer all the following Questions (10MX 5=50Marks)

11. With neat sketches explain BICMOS fabrication in an n-well process. [10M]

OR

12 Illustrate the relationship between I_{ds} versus V_{ds} of MOSFET. [10M]
13 Draw the CMOS logic circuit and stick diagram for the NAND gate. [10M]

OR

14 Explain λ- based design rules for transistors, wires, contact cuts and vias. [10M]

15 Explain about Pseudo nMOS logic and clocked CMOS logic. [10M]

OR

16 a) Explain the concept of MOSFET as switches. [4M]
b) Derive the expression for time delays in case of MOSFETs. [6M]
17 Draw the schematic and explain the operation of Wallace tree Multiplier. [10M]

OR

18 a) Explain about serial access memories. [5M]
b) Explain about different types of ROM. [5M]
19 Explain the architecture of CPLD with neat diagram. [10M]

OR

20 a) Write about CMOS testing. [5M]
b) Explain about design strategies for testing. [5M]