Regulation R18 *Subject code: 2E6BB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A' Grade)

B.Tech VI Semester Supplementary Examinations, June/July 2023

Computer Architecture

(EEE)

Maximum Marks: 70 Date:03.07.2023 Duration: 3 hours

Note:
1. **This question paper contains two parts A and B.**
2. **Part A is compulsory which carries 20 marks. Answer all questions in Part A.**
3. **Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.**
4. **Each question carries 10 marks and may have a, b, c, d as sub questions.**

Part-A

All the following questions carry equal marks (10x2M=20 Marks)

1 Compare RISC with CISC?
2 Differentiate between Computer Architecture and Organization
3 What do you mean by memory hierarchy?
4 Why does increasing the capacity of cache tend to increase its hit rate?
5 Write the benefits of serial communication?
6 What is a priority interrupt?
7 What is the purpose of PUSH and POP instruction in microprocessor instruction set?
8 What is the difference between opcode and operand?
9 Define instruction level of pipelining?
10 How many segments are there in the pipeline?

Part-B

Answer All the following questions. (10MX 5=50Marks)

11 Explain briefly about float point representation and floating-point addition and subtraction algorithm. [10]

OR

12 A. What is the difference between a hardwired control unit and a micro programmed control unit? Explain the relative advantages of each. [5]
B. Explain the multi-bus organization of computer architecture? [5]

13 Define cache memory? Explain the various Mapping Techniques associated with cache memories. [10]

OR

14 A. What is virtual memory? Explain the steps involved in virtual memory address translation.[5]
B. What is memory Management hardware? Explain. [5]

15 Explain the operation of DMA using a block diagram. Give an example application of DMA data transfer. [10]

OR

16 What Bus arbitration and explain approaching methods? [10]

17 Explain the architecture of 8086 microprocessors with neat block diagram? [10]

OR

18 Explain memory segmentation in 8086 microprocessors? What are the advantages and disadvantages? [10]

19 What do you understand by Instruction Pipeline? Mention the stages of Pipeline. [10]

OR

20 Describe in detail about the functional units and the basic implementation scheme of MIPS with suitable diagram. [10]