



**B.Tech III Semester Regular/Supplementary Examinations, December 2025**

**COMPUTER ORGANIZATION AND ARCHITECTURE**

**(IT)**

**Maximum Marks: 60**

Date:24.12.2025

Duration: 3 hours

- Note:**
1. This question paper contains two parts A and B.
  2. Part A is compulsory which carries 10 marks. Answer all questions in Part A.
  3. Part B consists of 5 Units. Answer any one full question from each unit.
  4. Each question carries 10 marks and may have a, b, c, d as sub questions.

**Part-A**

All the following questions carry equal marks (10X1M=10 Marks)		Marks	CO	Bloom Tx
1.a)	List of functional units.	1M	1	Remember
b)	Write the basic CPU performance equation.	1M	1	Remember
c)	What is the role of PC in instruction execution.	1M	2	Remember
d)	What happens in the "decode" phase of instruction execution.	1M	2	Remember
e)	What is WAR hazard.	1M	3	Remember
f)	What is pipelining.	1M	3	Remember
g)	Which type of RAM is used in CPU cache.	1M	4	Remember
h)	How EPROM is erased.	1M	4	Remember
i)	Which bus carries control signals.	1M	5	Remember
j)	PCI is an example of which type of bus.	1M	5	Remember

**Part-B**

Answer All the following questions. (5X10M=50Marks)		Marks	CO	Bloom Tx
2	a) List and explain any six addressing modes with an example instruction.	5M	1	Understand
	b) Explain Booth's algorithm for multiplication of signed numbers.	5M	1	Understand
OR				
3	a) Explain the 2's complement multiplication of an unsigned number using 5 bit registers	5M	1	Understand
	b) Design a 4 bit carry look ahead adder.	5M	1	Apply
4	a) Explain the generation of control signals in a CPU.	5M	2	Understand
	b) Explain the characteristics of CISC style processors.	5M	2	Understand
OR				
5	a) Explain in detail the data path for a single cycle processor.	5M	2	Understand
	b) Explain the major hardware components of processing unit.	5M	2	Understand
6	a) Classify the types of pipeline hazards with suitable example.	5M	3	Understand
	b) Explain the performance metrics of a pipeline.	5M	3	
OR				

7	a) Explain how the memory delay affects the pipeline performance.	5M	3	Understand
	b) Explain the challenges of pipelining in CISC processors.	5M	3	Understand
8	a) Explain the working of DMA controller.	5M	4	Understand
	b) Differentiate between. i) Static RAM vs Dynamic RAM ii) PROM vs EEPROM	5M	4	Understand
OR				
9	a) Explain the concept of virtual memory.	5M	4	Understand
	b) Explain the different levels of cache memory ( L1, L2, L3 ).	5M	4	Understand
				Understand
10	a) Explain the working of a typical I/O interface circuit with a neat diagram.	6M	5	Understand
	b) Compare any two features of the interconnection standards.	4M	5	
OR				
11	a) Compare the SCSI and SAS interface standards.	5M	5	Understand
	b) Explain in detail the interrupt driven I/O mechanism.	5M	5	Understand