R22 Regulation *Subject code:4E3ED*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech III Semester Regular/Supplementary Examinations, December 2025

COMPUTER ARCHITECTURE AND ORGANIZATION

(Common to CSE & CSE(AIML))

Maximum Marks: 60 Date:24.12.2025 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 10 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10X1M=10 Marks)		Marks	CO	BTL
1.a)	List any four types of computer registers.	1M	1	L1
b)	Define instruction cycle.	1M	1	L1
c)	Define hardwired control unit.	1M	2	L1
d)	What is microprogram control?	1M	2	L1
e)	List any two types of logical and bit manipulation instructions.	1M	3	L1
f)	Give an example of decimal representation.	1M	3	L1
g)	Why is cache memory faster than main memory?	1M	4	L1
h)	What is priority interrupt?	1M	4	L1
i)	What are CISC characteristics?	1M	5	L1
j)	List the key features of an array processor.	1M	5	L1

Part-B

Answer All the following questions. (5X10M=50Marks)		Marks	CO	BTL
2	a) Explain about computer design and architecture. b) Describe the instruction cycle and its phases.	5M 5M	1	L2
	OR			
3	Explain about different types of basic computer registers with common bus system.	10M	1	L2
4	Analyze the different functionalities of 8086 microprocessor architecture.	10M	2	L3
	OR			
5	a) Discuss the physical address formation in 8086. b) Draw the read and write cycle timing diagrams of 8086 in minimum mode.	5M 5M	2	L2
6	a) Explain the concept of floating - point addition and subtraction. b) Distinguish between fixed point representation and floating-point representation.	5M 5M	3	L2

	OR			
7	a) Represent the number (+46.5)10 as a floating-point binary number with 24 bits. The normalized fraction mantissa has 16 bits and the exponent has 8 bits. b) Explain Booths multiplications algorithm with an example.	5M 5M	3	L3
8	a) Explain the different types of peripheral devices with suitable examples. b) Explain asynchronous data transfer techniques with timing diagrams.	5M 5M	4	L2
	OR			
9	a) Explain Set Associative mapping for organizing cache memory. b) Consider the following reference string: 1 2 3 4 1 2 5 1 2 3 4 5, apply FIFO page replacement algorithm and calculate number of page faults by considering 3 frames.	5M 5M	4	L3
10	a) State and explain the characteristics of multi-processors. b) Explain instruction pipeline stages with a neat diagram.	5M 5M	5	L2
	OR			
11	a) Explain about arithmetic pipelining with an example. b) Explain RISC characteristics with its advantages.	5M 5M	5	L2