



R20 Regulation

Subject code: 3P4FB

# TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech IV Semester Supplementary Examinations, December 2025

## COMPUTER ORGANIZATION (IT)

Maximum Marks: 70

Date: 18.12.2025

Duration: 3 hours

- Note:
1. This question paper contains two parts A and B.
  2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
  3. Part B consists of 5 Units. Answer any one full question from each unit.
  4. Each question carries 10 marks and may have a, b, c, d as sub questions.

### Part-A

| All the following questions carry equal marks (10X2M=20 Marks) |   | Marks | CO | BTL |
|--|---|-------|----|-----|
| 1  | Define Digital Computer.                                    | 2M    | 1  | L1  |
| 2  | Compare Hardwired control and Micro programmed control.     | 2M    | 1  | L1  |
| 3  | What are the advantages of DMA?                             | 2M    | 2  | L1  |
| 4  | Explain different type of Hardware and Software interrupts. | 2M    | 2  | L1  |
| 5  | Explain content addressable memory.                         | 2M    | 3  | L1  |
| 6  | Explain about auxiliary memory in memory organization.      | 2M    | 3  | L1  |
| 7  | Discuss the purpose of INTR in 8086 micro-processor.        | 2M    | 4  | L1  |
| 8  | Write the memory Read statement in 8086 micro-processor.    | 2M    | 4  | L1  |
| 9  | Explain ROR and ROL 8086 instruction.                       | 2M    | 5  | L1  |
| 10   | Explain stoning instruction of 8086.                        | 2M    | 5  | L1  |

### Part-B

| Answer All the following questions. (5X10M=50Marks) |   | Marks | CO | BTL |
|---|---|-------|----|-----|
| 11  | Draw the flow chart for interrupt cycle of a basic computer and explain.  | 10M   | 1  | L2  |
| OR  |   |       |    |     |
| 12  | Explain micro programmed address sequencer with neat diagram.   | 10M   | 1  | L2  |
| 13  | A CPU with 20 MHz clock is connected to a memory unit whose access time is 40ns. Formulate a read and write timing diagrams, using a READ strobe and a WRITE strobe. Include the address in the timing diagram. | 10M   | 2  | L2  |
| OR  |   |       |    |     |
| 14  | Draw the block diagram of DMA controller and DMA Transfer of data with relevant information.  | 10M   | 2  | L2  |
| 15  | Describe associative mapping in cache memory.   | 10M   | 3  | L2  |
| OR  |   |       |    |     |
| 16  | Explain virtual memory concept and how the logical address is mapped to the physical address with numerical example.  | 10M   | 3  | L2  |

|    |   |     |   |    |
|----|---|-----|---|----|
| 17 | Draw and explain the PIN configuration of 8086 microprocessor.  | 10M | 4 | L2 |
|    | OR  |     |   |    |
| 18 | What is the difference between effective address and physical address of an instruction in 8086? Explain with an example. | 10M | 4 | L2 |
| 19 | Write a program 8086 AL, for displaying the string using library functions  | 10M | 5 | L2 |
|    | OR  |     |   |    |
| 20 | Discuss about evaluation of arithmetic expression in 8086 assembly language programming.                                  | 10M | 5 | L2 |