R20 Regulation *Subject code: 3P4EB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech IV Semester Supplementary Examinations, December 2025

COMPUTER ORGANIZATION AND ARCHITECTURE
(CSE)

Maximum Marks: 70 Date: 18.12.2025 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10X2M=20 Marks)		Marks	CO	BTL
1	Draw the block diagram of Digital computer.	2M	1	L1
2	What is an instruction cycle?	2M	1	L1
3	Define Addressing modes.	2M	2	L1
4	Write about MOV instruction.	2M	2	L1
5	Write the 2's complement of 1011011.	2M	3	L1
6	Give a reason for the use of guard bits.	2M	3	L1
7	What is cache memory?	2M	4	L1
8	Why IO devices cannot be directly be connected to the system bus?	2M	4	L1
9	What is Pipelining.	2M	5	L1
10	Define Critical Section.	2M	5	L1

Part-B

Answer All the following questions. (5X10M=50Marks)		Marks	CO	BTL
11	Explain about different types of instruction codes with example.	10M	1	L2
	OR			
12	Explain about instruction cycle with neat diagram.	10M	1	L2
13	a) Write the differences between hard wired control and micro programmed control. b) State any four features of 8086 microprocessor.	5M 5M	2	L2
	OR			
14	Draw the PIN configuration of 8086 microprocessor and explain about the PINs.	10M	2	L2
15	a) What are the various ways of representing negative numbers? Explain with example. b) Perform the arithmetic operation in binary using 2's complement representation (+42) + (-13) (ii) (-42) – (-13)	5M 5M	3	L2
	OR			

16	With an example, explain Booth Multiplication algorithm.	10M	3	L2
17	a) What is DMA? Explain. b) Explain about serial communication.	5M 5M	4	L2
	OR			
18	a) Draw the neat sketch of memory hierarchy and explain the need of cache memory. b) Explain about direct and set associative map technique in cache.	5M 5M	4	L2
19	a) Write the major characteristics of RISC processors b) Draw a space-time diagram for a four-segment pipeline showing the time it takes to process six tasks and explain.	5M 5M	5	L2
	OR			
20	a) Explain the Vector Processing in detail. b) Write about Array processing.	5M 5M	5	L2