R20 Regulation *Subject code:3P3FA*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech III Semester Supplementary Examinations, December 2025

DIGITAL LOGIC DESIGN

(IT)

Maximum Marks: 70 Date: 19.12.2025 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10X2M=20 Marks)		Marks	CO	BTL
1	What is Gray code? Give one example.	2M	1	L1
2	Find the 2's complement of 11101010, 01111110.	2M	1	L1
3	What is the prime implicant chart?	2M	2	L1
4	What is mean by minterm and maxterm?	2M	2	L1
5	Write the differences between combinational and sequential circuits.	2M	3	L1
6	Define Decoder? List out the applications of it?	2M	3	L1
7	What are applications of Flip-Flop?	2M	4	L1
8	What are the basic types of shift registers?	2M	4	L1
9	What is state diagram?	2M	5	L1
10	Compare Mealy and Moore machines.	2M	5	L1

Part-B

Answer All the following questions. (5X10M=50Marks)		Marks	CO	BTL
11	a) Convert the given gray code number to equivalent binary 0010010111110010 b) Convert $(A0F9.0DC)_{16}$ to decimal, binary, octal	5M 5M	1	L2
	OR			
12	Perform 2's & 1's complement arithmetic for given numbers -25 and 14.	10M	1	L2
13	Reduce using mapping the expression f= πM(2,8,9,10,11,12,14) and Implement the real minimal expression in universal logic.	10M	2	L2
	OR			
14	a) Simplify the following Boolean expressions using the Boolean theorems. (i) (A+B+C) (B′+C) + (A+D) (A′+C) (ii) (A+B) (A+B′) (A′+B) b) Why a NAND and NOR gates are known as universal gates? Simulate all the basic Gates.	5M 5M	2	L2
15	a) Explain the differences between a MUX and a DEMUX. b) Realize 16-input multiplexer by cascading of two 8-input multiplexers	5M 5M	3	L2
	OR			

16	Design 2-bit digital comparator and explain with neat sketch.	10M	3	L2
17	What is meant by Edge triggered? Differentiate SR-FF and JK-FF with their functional operation and excitation tables.	10M	4	L2
	OR			
18	Design a mod-12 Ripple counter using T flip flops and explain its operation.	10M	4	L2
19	Draw the state diagram, state table for sequence detector circuit to detect 1110	10M	5	L2
	OR			
20	What are the capabilities and limitations of finite state machines? Discuss.	10M	5	L2