R20 Regulation *Subject code: 3P3EC*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech III Semester Supplementary Examinations, December 2025

LOGIC CIRCUITS DESIGN

(Common to CSE & CSE (AI & ML)

Maximum Marks: 70 Date: 19.12.2025 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10X2M=20 Marks)		Marks	CO	BTL
1	What are the three main Boolean operators?	2M	1	L1
2	Convert octal number 3600 into decimal number.	2M	1	L1
3	State the limitations of K-Map.	2M	2	L1
4	Draw the block diagram of 2-4 and 3-8 decoders.	2M	2	L1
5	What is a flip-flop? Write down the characteristic equation of S-R flipflop.	2M	3	L1
6	Differentiate combinational and sequential logic circuits.	2M	3	L1
7	What is the designation of registers?	2M	4	L1
8	What are the Micro operations?	2M	4	L1
9	Define RAM and types.	2M	5	L1
10	Define address and word.	2M	5	L1

Part-B

Answer All the following questions. (5X10M=50Marks)		Marks	CO	BTL
11	a) Simplify the following expression Y = (A + B) (A + C') (B' + C'). b) Convert the octal numbers into binary, decimal, BCD and Hexadecimal numbers(3600)octal, (1200)octal, (0200)octal,(0777)octal	5M 5M	1	L2
	OR			
12	a) Find (72532 - 03250) using 9's and 10's complement. b) Explain about different logical gates and universal gates.	5M 5M	1	L2
13	a) Simplify the Boolean expression using K-map F(A,B,C,D,E)= Σm(0,1,2,4,5,6,8,9,12,13,14). b) Explain about multiplexer and demultiplexers.	5M 5M	2	L2
	OR			
14	Explain 8:1 Multiplexer and 4:1 Demultiplexer.	10M	2	L2
15	Write the differences between (a) Combinational circuits and sequential circuit. (b) Flip- flops and Latches	5M 5M	3	L2
	OR			

16	Write the different kinds of flip-flops. Explain the SR flip-flop.	10M	3	L2
17	a) With a neat diagram explain in detail about ALU(Arithmetic Logic Shift Unit). b) Design and explain a 4-bit binary parallel Adder/Subtractor.	6M 4M	4	L2
	OR			
18	With a neat diagram construct a bus system for 4 registers using multiplexers and also using tri state buffers.	10M	4	L2
19	Explain about Programmable array Logic (PAL) and Programmable Logic array (PLA).	10M	5	L2
	OR			
20	Explain about sequential Programmable device and types.	10M	5	L2