R18 Regulation *Subject code:2P4DD*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech IV Semester Supplementary Examinations, December 2025

LINEAR & DIGITAL IC APPLICATIONS
(ECE)

Maximum Marks: 70 Date: 23.12.2025 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10X2M=20 Marks)		Marks	CO	BTL
1	List features of 741 op-amp.	2M	1	L1
2	What is Zero crossing detector?	2M	1	L1
3	List various applications of IC 555 Timer.	2M	2	L1
4	List the features of IC 555.	2M	2	L1
5	Define resolution and settling time.	2M	3	L1
6	Mention the advantages and disadvantages of Dual slope ADC.	2M	3	L1
7	Write a short note on priority encoder.	2M	4	L1
8	Sketch the 4x16 decoder using 74LS138 IC's.	2M	4	L1
9	How to convert JK flipflop to D flipflop?	2M	5	L1
10	Define ROM and programmable logic array. Differentiate them.	2M	5	L1

Part-B

Answer All the following questions. (5X10M=50Marks)		Marks	CO	BTL
11	Draw the circuit diagram of a two input non-inverting summing amplifier and derive the expression for the output voltage.	10M	1	L2
	OR			
12	Explain the operation of Integrator and plot its output waveforms for different inputs.	10M	1	L2
13	Draw the circuit diagram of Wein Bridge oscillator. Derive the expression for its gain and frequency of oscillations.	10M	2	L2
	OR			
14	Explain the monostable operation of the 555 timer and derive the expression for the period of a pulse generated by the Timer.	10M	2	L2
15	Explain the operation of the fastest analog to digital converter. What is the main draw back of this converter? Compare this converter with other types.	10M	3	L2

	OR			
16	Explain the principle of operation of Successive Approximation ADC.	10M	3	L2
17	Explain about TTL driving CMOS and CMOS driving TTL with noise margin levels.	10M	4	L2
	OR			
18	Explain with neat diagram interfacing of TTL gate driving CMOS and CMOS driving TTL Gates.	10M	4	L2
19	Differentiate between ripple counter and synchronous counter? Design a 3-bit synchronous counter.	10M	5	L2
	OR			
20	Design and implement 4-bit synchronous down counter using IC.	10M	5	L2