R22 Regulation *Subject code: 4P6DA*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech VI Semester Supplementary Examinations, November 2025

DIGITAL DESIGN THROUGH VERILOG HDL

(ECE)

Maximum Marks: 60 Date:13.11.2025 Duration: 3 hours

Note:
1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 10 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10X1M=10 Marks)		Marks	CO	Bloom Tx
1.a)	Write the different levels of design description in Verilog.	1M	CO1	BT1
b)	Write about white space character with an example.	1M	CO1	BT1
c)	What are tristate gates?	1M	CO2	BT1
d)	Write a note on AND/OR Gates.	1M	CO2	BT1
e)	What are the logical operators in Verilog?	1M	CO3	BT1
f)	Design the circuit diagram for CMOS NOR gate.	1M	CO3	BT2
g)	Give the syntax of "always" construct.	1M	CO4	BT1
h)	What are the delta delay and #0 delay in Verilog?	1M	CO4	BT1
i)	What are local parameters?	1M	CO5	BT1
j)	List out file based Tasks in Verilog HDL.	1M	CO5	BT2

Part-B

Answer All the following questions. (5X10M=50Marks)		Marks	CO	Bloom Tx
2	Explain the ASIC design Flow briefly. Explain Role of HDL in ASIC design flow.	10M	CO1	BT2
	OR			
3	Write about scalars and vectors in verilog modules and their differences with examples.	10M	CO1	BT3
4	a) Describe the following relevant to gate level modelling with necessary syntax and example. i. Gate delays ii. Array of instances b) Give a gate level description of a 2-4 decoder circuit with relevant logic diagram and Verilog HDL source code.	5M 5M	CO2	BT3
	OR			
5	a) Describe the following relevant to gate level modelling with necessary syntax and example. i. Rise, Fall and Turn off Delays ii. Strengths and contention resolution b) Present the gate level description of a SR Flip flop circuit with relevant logic diagram and Verilog HDL source code.	5M 5M	CO2	BT3

6	a) Explain Carry Look Ahead adder. Write a Verilog code with data flow style program for carry look ahead adder. b) What is continuous assignment? Discuss the rules of continuous assignment.	7M 3M	CO3	BT4
	OR			
7	a) Draw and explain the circuit diagram of CMOS switch with a program. b) Explain the Bi-directional Switches and Resistive Switches.	5M 5M	CO3	BT3
8	Explain the following. a) Procedural Continuous Assignments b) Procedural Assignments	5M 5M	CO4	BT3
	OR			
9	a) Write the Verilog code for the AOI circuit using Behavioral modeling. b) Write a verilog code for up counter using behavioral model.	5M 5M	CO4	BT4
10	a) Discuss about compiler directives in verilog with syntax and one example for each. b) Distinguish Tasks and Function with examples.	5M 5M	CO5	BT4
	OR			
11	a) Define user defined primitives with their syntax. Give an example of 4 to 1 multiplexer built using UDPs. b) Write verilog code for edge triggered D- Flip Flop with clear input using UDP.	5M 5M	CO5	BT4