R22 Regulation *Subject code:4E6DC*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech VI Semester Supplementary Examinations, November 2025

VLSI DESIGN

(ECE)

Maximum Marks: 60 Date:11.11.2025 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 10 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10X1M=10 Marks)		Marks	CO	Bloom Tx
1.a)	Give the advantages of BiCMOS process compared with the CMOS.	1M	CO1	BT2
b)	Define g_m of MOS transistor.	1M	CO1	BT1
c)	State the purpose of design rule.	1M	CO2	BT1
d)	List the advantages of CMOS.	1M	CO2	BT1
e)	Enlist the three sources of wiring capacitance.	1M	CO3	BT1
f)	What are the issues involved in driving large capacitive loads in VLSI circuits?	1M	CO3	BT2
g)	Why barrel shifter is very useful in the designing of arithmetic circuits?	1M	CO4	BT2
h)	Mention about SRAM and its usage.	1M	CO4	BT1
i)	Write the draw backs of PLAs.	1M	CO5	BT1
j)	What is a test vector? How are they used in chip level testing?	1M	CO5	BT2

Part-B

Answer All the following questions. (5X10M=50Marks)		Marks	CO	Bloom Tx
2	a) Discuss the Basic Electrical Properties of MOS and BiCMOS Circuits. b) Write about CMOS fabrication in a n-well process with a diagram.	5M 5M	CO1	BT3
	OR			
3	a) Derive the relationship between I_{ds} and V_{ds}. b) Define threshold voltage? Derive the V_t equation for MOS transistor.	5M 5M	CO1	BT3
4	Design a symbolic diagram and stick diagram for 2 input NAND gate and 2 input NOR gate.	10M	CO2	BT4
	OR			
5	Explain in detail about Layout design rules and design for CMOS inverter with neat layout design rules.	10M	CO2	BT4
6	Discuss about the logics implemented in gate level design and explain the switch logic implementation for a four by one multiplexer.	10M	CO3	BT3
	OR			
7	What are the alternate gate circuits available? Explain any one of item with suitable sketch by taking NAND gate as an example.	10M	CO3	BT3

8	a) Describe the working principle of Ripple carry adder using Transmission Gates. b) Design a shift register with the dynamic latch operated by a two-phase clock.	5M 5M	CO4	BT4
	OR			
9	a) Draw the structure of a 4×4 static RAM and explain its operation. b) Draw the circuit diagram of four transistor DRAM cell with storage nodes.	5M 5M	CO4	BT4
10	a) Compare CPLD and FPGA. b) Discuss the different methods of programming of PALs.	5M 5M	CO5	BT4
	OR			
11	Why the chip testing is needed? At what levels testing a chip can occur? Discuss the chip level test techniques.	10M	CO5	BT4