R20 Regulation *Subject code: 3P6DD*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech VI Semester Supplementary Examinations, November 2025

VLSI DESIGN

(ECE)

Maximum Marks: 70 Date: 13.11.2025 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10X2M=20 Marks)		Marks	CO	BTL
1	What is Moore's Law.	2M	1	L1
2	Define Threshold voltage.	2M	1	L1
3	List the various color coding used in stick diagram	2M	2	L1
4	Sketch a stick diagram for CMOS inverter.	2M	2	L1
5	What is pass transistor logic?	2M	3	L1
6	Define fan out.	2M	3	L1
7	What are different types of Serial Access Memories?	2M	4	L1
8	Draw the circuit diagram of full adder.	2M	4	L1
9	What are programmable logic devices?	2M	5	L1
10	Define Stuck open faults.	2M	5	L1

Part-B

Answer All the following questions. (5X10M=50Marks)		Marks	CO	BTL
11	Explain about the CMOS Inverter with characteristics.	10M	1	L2
	OR			
12	Illustrate the relationship between I_{ds} versus V_{ds} of MOSFET.	10M	1	L2
13	Draw the CMOS logic circuit, stick diagram and layout for the following Boolean expression F = [D+A.(B+C)]'.	10M	2	L2
	OR			
14	a) Explain about 2µm CMOS design rules for wires, transistors and transistors. b) Write the demerits of Scaling.	5M 5M	2	L2
15	Explain in detail about Dynamic CMOS logic and CMOS Domino logic gates with suitable example.	10M	3	L2
	OR			
16	a) Describe the sources of wiring capacitance. b) List the logical constraints of layers.	6M 4M	3	L2
17	a) Draw the logic diagram of zero/one detector and explain its operation. b) Explain about ALU subsystem.	5M 5M	4	L2

	OR			
18	a) Describe briefly 4-bit parallel adder. b) Draw and explain the operation of SRAM cell.	5M 5M	4	L2
19	Explain the architecture of FPGA with neat diagram.	10M	5	L2
	OR			
20	Discuss chip level testing techniques.	10M	5	L2