



R20 Regulation

Subject code: 3E5DA

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech V Semester Supplementary Examinations, November 2025

DIGITAL DESIGN THROUGH VERILOG HDL (ECE)

Maximum Marks: 70

Date: 14.11.2025

Duration: 3 hours

- Note:
1. This question paper contains two parts A and B.
 2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
 3. Part B consists of 5 Units. Answer any one full question from each unit.
 4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10X2M=20 Marks)		Marks	CO	BTL
1	List the advantages of Verilog HDL.	2M	1	L1
2	Write strengths.	2M	1	L1
3	Classify Gate Types.	2M	2	L1
4	Define gate delay.	2M	2	L1
5	Write about ternary operator with example.	2M	3	L1
6	Write the CMOS inverter Verilog code.	2M	3	L1
7	Define fork join block.	2M	4	L1
8	Write the syntax for a while loop.	2M	4	L1
9	Define task.	2M	5	L1
10	Write a syntax for \$monitor.	2M	5	L1

Part-B

Answer All the following questions. (5X10M=50Marks)		Marks	CO	BTL
11	Illustrate the application of Verilog HDL by discussing the various modeling styles and providing examples for each.	10M	1	L2
OR				
12	Explain about Lexical tokens in Verilog.	10M	1	L2
13	Create a comprehensive plan for constructing full subtractor by using Gate level modeling.	10M	2	L2
OR				
14	Design and develop 3to8 decoder using 2 to 4 decoder in gatelevel model.	10M	2	L2
15	Design and develop 2 Input-CMOS NOR in switch level modeling with test bench and results.	10M	3	L2
OR				
16	Design and develop full adder using two half adders in dataflow modeling with simulation results.	10M	3	L2

17	formulate a Verilog code for blocking and Non-blocking statements with examples	10M	4	L2
	OR			
18	Synthesize a complex scenario that requires the use of if and else if constructs in Verilog with example.	10M	4	L2
19	a) Analyze the \$strobe task in Verilog with an example. b) Distinguish the significance of compiler directives in Verilog.	5M 5M	5	L2
	OR			
20	Define UDP and explain each types of UDP with an example.	10M	5	L2