R18 Regulation *Subject code:2P5DB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech V Semester Supplementary Examinations, November 2025

VLSI DESIGN

(ECE)

Maximum Marks: 70 Date: 20.11.2025 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10X2M=20 Marks)		Marks	CO	BTL
1	What is body effect?	2M	1	L1
2	Define figure of merit.	2M	1	L1
3	Explain different MOS layers.	2M	2	L1
4	What is stick diagram?	2M	2	L1
5	List the sources of wiring capacitance.	2M	3	L1
6	Define Switch logic.	2M	3	L1
7	What are different types of Serial Access Memories	2M	4	L1
8	Draw the circuit diagram of full adder.	2M	4	L1
9	Write the abbreviation of FPGA.	2M	5	L1
10	Define controllability.	2M	5	L1

Part-B

Answer All the following questions. (5X10M=50Marks)		Marks	CO	BTL
11	With neat sketches explain CMOS fabrication in an n-well process.	10M	1	L2
	OR			
12	Explain the operation of NMOS enhancement transistor.	10M	1	L2
13	Sketch the schematic, stick diagram and layout for the Boolean expression Y = (AB + C)'.	10M	2	L2
	OR			
14	Draw the CMOS logic circuit, stick diagram and layout for the following Boolean expression F = [A.(B+C)]'.	10M	2	L2
15	What are the alternate gate circuits available? Explain any one of them with suitable sketch by taking NAND gate as an example.	10M	3	L2
	OR			
16	What are the issues involved in driving large capacitive loads in VLSI circuits? Explain.	10M	3	L2
17	Draw the basic circuit diagram of static RAM cell and explain its read and write operation.	10M	4	L2

	OR			
18	a) Explain about serial access memories. b) Explain about different types of ROM.	5M 5M	4	L2
19	Explain the architecture of FPGA with neat diagram.	10M	5	L2
	OR			
20	Discuss chip level testing techniques.	10M	5	L2