R18 Regulation *Subject code:2P4BB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech IV Semester Supplementary Examinations, April 2025

DIGITAL LOGIC DESIGN

(EEE)

Maximum Marks: 70 Date: 08.05.2025 Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c as sub questions.

Part-A

	All the following questions carry equal marks (10X2M=20 Marks)	Marks	CO	BTL
1	What is Gray code?	2M	1	L1
2	How do you obtain dual of an expression?	2M	1	L1
3	What is the prime implicant chart?	2M	2	L1
4	Define the full subtractor.	2M	2	L1
5	Write the differences between combinational and sequential circuits.	2M	3	L1
6	What is race around condition?	2M	3	L1
7	Differentiate between RAM and ROM.	2M	4	L1
8	What are drawbacks of ripple counters?	2M	4	L1
9	What are finite state machines?	2M	5	L1
10	Define sequential machine.	2M	5	L1

Part-B

	Answer All the following questions. (5X10M=50Marks)	Marks	CO	BTL
11	a) Convert the gray number 101101 into decimal, hex, octal	5M	1	L2
	b) Perform the subtraction in BCD using 9's complement method for 592.6-887.9	5M		
	OR			
12	Expand (A+D')(A+C')(A'+B)(A'+B+C) into max terms and min terms.	10M	1	L2
13	Minimize the following expression using K-map and realize using NAND Gates. F (A,B,C,D) = m (0,1,2,9,11 +d(8,10,14,15).	10M	2	L2
	OR			
14	Explain about Multiplexer .Design a 32X1 multiplexer using 4x1 multiplexer.	10M	2	L2
15	Explain the circuit operation with a neat logic diagram.	10M	3	L2
	OR			
16	a) Draw a neat circuit diagram of positive edge triggered D flip-flop and explain its operation.	5M	3	L2
	b) Convert D flip-flop into JK flip-flop.	5M		

<table>
<tr><td>17</td><td>What do you mean by universal shift register? Draw and explain its circuit diagram and operation.</td><td>10M</td><td>4</td><td>L2</td></tr>
<tr><td></td><td>OR</td><td></td><td></td><td></td></tr>
<tr><td>18</td><td>Design a 4-bit up/down Synchronous BCD counter using T flip flops.</td><td>10M</td><td>4</td><td>L2</td></tr>
<tr><td>19</td><td>Construct the compatibility graph and obtain the minimal cover table for sequential machine given by state table below.
<table>
<tr><th rowspan="2">PS</th><th colspan="2">NS,Z</th></tr>
<tr><th>I_1</th><th>I_2</th></tr>
<tr><td>A</td><td>E, 1</td><td>B, 1</td></tr>
<tr><td>B</td><td>F, 1</td><td>A, 1</td></tr>
<tr><td>C</td><td>E, -</td><td>C, 1</td></tr>
<tr><td>D</td><td>F, 0</td><td>D, 1</td></tr>
<tr><td>E</td><td>C, 0</td><td>C, 1</td></tr>
<tr><td>F</td><td>D, -</td><td>B, 1</td></tr>
</table></td><td>10M</td><td>5</td><td>L2</td></tr>
<tr><td></td><td>OR</td><td></td><td></td><td></td></tr>
<tr><td>20</td><td>a) What are the Moore and Mealy machines? Compare them.
b) What are the capabilities and limitations of finite state machines? Explain.</td><td>5M
5M</td><td>5</td><td>L2</td></tr>
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