R22 Regulation *Subject code: 4E3FB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech III Semester Regular/Supplementary Examinations, December 2024

COMPUTER ORGANIZATION AND ARCHITECTURE

(IT)

Maximum Marks: 60 Date:11.12.2024 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 10 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

	Part-A	CO	Bloom Tx
All the following questions carry equal marks	(10X1M=10 Marks)		
1.a)	What are different types of computers?	1	L1
b)	Write is the Reduced Instruction Set Computer?	1	L1
c)	What is RISC vs CISC?	2	L1
d)	What is fetch policy in computer architecture?	2	L1
e)	What is data dependence with an example?	3	L1
f)	Write the one issue of Pipeline organization.	3	L1
g)	What is RAM?	4	L1
h)	What are the three types of secondary storage?	4	L1
i)	What is PCI?	5	L1
j)	What is SATA?	5	L1
	Part-B		
Answer All the following questions.	(5X10M=50Marks)	CO	Bloom Tx
2	Design and explain 4-bit adder-subtractor and 4-bit arithmetic circuit to perform addition and subtraction using full adders. [10M]	1	L2
	OR		
3	Dividend A=01110 Divisor B=10001. Explain flowchart for divide operation. [10M]	1	L2
4	What is Instruction Cycle and explain in detail about the types of Instruction Cycle. [10M]	2	
	OR		
5	Describe the control unit organization with a separate Encoder and Decoder functions in a hardwired control. [10M]	2	L6
6	Describe in detail about pipeline processing. [10M]	3	L6
	OR		
7	Explain in detail about the CISC pipeline vector processing. [10M]	3	L2

8	Explain Cache with associative and two-way Set- Associative mapping with a line size of 4 bytes. [10M]	4	L2
	OR		
9	Describe the use of DMA controllers in a computer system with a neat block diagram. [10M]	4	L6
10	Explain in detail about the interconnection standards. [10M]	5	L2
	OR		
11	Discuss in detail about the Program Controlled I/O Interrupts. [10M]	5	L6