R20 Regulation *Subject code:3P4BB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech IV Semester Supplementary Examinations, December 2024

DIGITAL ELECTRONICS
(Electrical and Electronics Engineering)

Maximum Marks: 70 Date:05.12.2024 Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10X2M=20) Marks)		CO	Bloom Tx
1	What is Gray code?	1	L1
2	How do you obtain dual of an expression?	1	L1
3	What are don't cares?	2	L1
4	State De Morgan's theorem.	2	L1
5	Define the full subtractor.	3	L1
6	List the applications of Multiplexers	3	L1
7	Write the differences between combinational and sequential circuits.	4	L1
8	Define the ring counter.	4	L1
9	What are finite state machines?	5	L1
10	Define sequential machine.	5	L1

Part-B

Answer All the following questions. (5X10M=50Marks)		CO	Bloom Tx
11	A) Given the 8 bit data word 11011011, generate the 12 bit composite word for the Hamming code that corrects and detects single errors. [5M] B) Convert $(A0F9.0DC)_{16}$ to decimal, binary, octal [5M]	1	L3
	OR		
12	A) Convert the gray number 101101 into decimal, hex, octal [5M] B) Perform the subtraction in BCD using 9's complement method for 592.6-887.9 [5M]	1	L3
13	Minimize the following expression using K-map and realize using NAND Gates. F (A,B,C,D) = $\sum$m (0,1,2,9,11) +d(8,10,14,15). [10M]	2	L3
	OR		
14	Expand (A+D')(A+C')(A'+B)(A'+B+C) into max terms and min terms. [10M]	2	L2
15	Draw the circuit diagram of J-K flip flop with NAND gates and explain its operation with the help of truth table. How race around condition is eliminated. [10M]	3	L3

	OR		
16	A) Design a combinational circuit to produce the 2's complement of a 4-bit binary number. [7M] B) Compare combinational circuits and sequential circuits. [3M]	3	L4
17	Design a synchronous 3-bit Up-down counter using JK FFs [10M]	4	L4
	OR		
18	A) Draw the logic diagram of a SR latch using NOR gates. Explain its Operation using excitation table. [5M] B) Convert D flip-flop into T and JK flip-flops. [5M]	4	L3
19	Explain about sequential circuits, state table and state diagram [10M]	5	L2
	OR		
20	Explain about Mealy machine with circuit diagram [10M]	5	L2