R20 Regulation *Subject code:3P3FA*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech III Semester Supplementary Examinations, December 2024

DIGITAL LOGIC DESIGN

(Information Technology)

Maximum Marks: 70 Date:06.12.2024 Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10X2M=20) Marks)		CO	Bloom Tx
1	What is Gray code?	1	L1
2	Convert the number $(D9F.CE)_{16}$ into decimal.	1	L1
3	What are don't cares?	2	L1
4	Define the full subtractor.	2	L1
5	Compare latch and flip flop.	3	L1
6	List the applications of Multiplexers.	3	L1
7	What are applications of Flip-Flop?	4	L1
8	What are the basic types of shift registers?	4	L1
9	What is state diagram?	5	L1
10	Compare Mealy and Moore machines.	5	L1

Part-B

Answer All the following questions. (5X10M=50Marks)		CO	Bloom Tx
11	A. Convert the gray number 101101 into decimal, hex, octal. [5M] B. Perform the subtraction in BCD using 9's complement method for 592.6-887.9 [5M]	1	L2
	OR		
12	Generate hamming code sequence for given 11-bit message 01101110101. [10M]	1	L2
13	Simplify the expression $F(A,B,C,D)=A\bar{B}+AB\bar{D}+ABD+\bar{A}\bar{C}\bar{D}+\bar{A}B\bar{C}$ and implement with NAND gates only. [10M]	2	L2
	OR		
14	Reduce the expression using k map $F(A, B, C, D, E) = \Sigma(0,1, 2, 3, 5,7,8,9,10,12,13)$ and implement the real minimal expression in universal logic. [10M]	2	L2
15	Explain the priority encoder with a neat logic diagram. [10M]	3	L2
	OR		

16	Design 2-bit digital comparator and explain with neat sketch. [10M]	3	L2
17	What is meant by Edge triggered? Differentiate SR-FF and JK-FF with their functional operation and excitation tables. [10M]	4	L2
	OR		
18	Design a 4-bit up/down Synchronous BCD counter using T flip flops. [10M]	4	L2
19	Draw the state diagram, state table for sequence detector circuit to detect 1110. [10M]	5	L2
	OR		
20	What are the capabilities and limitations of finite state machines? Discuss. [10M]	5	L2