R20 Regulation *Subject code: 3P3EC*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech III Semester Supplementary Examinations, December 2024

LOGIC CIRCUITS DESIGN

(Common to CSE & CSE(AI&ML))

Maximum Marks: 70 Date:06.12.2024 Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

	Part-A		
All the following questions carry equal marks (10X2M=20) Marks)		CO	Bloom Tx
1	State De Morgan's theorem.	1	L1
2	Reduce A (A + B).	1	L1
3	Write the truth table of half adder.	2	L1
4	What is a K- map?	2	L1
5	Define a) Flip flop b) Latch	3	L1
6	Define register and RTL.	3	L1
7	List the arithmetic micro-operations and logic micro-operations.	4	L1
8	Write about three state bus buffer.	4	L1
9	What is the function of RAM?	5	L1
10	What is Sequential programable Device?	5	L1
	Part-B		
Answer All the following questions. (5X10M=50Marks)		CO	Bloom Tx
11	A.Simplify the following expression Y = (A + B) (A + C') (B' + C').[5M] B.Convert the octal numbers into binary, decimal, BCD and Hexadecimal numbers(3600)octal,(1200)octal,(0200)octal,(0777)octal [5M]	1	L3
	OR		
12	A.Find (72532 - 03250) using 9's and 10's complement. [5M] B.explain about different logical gates and universal gates? [5M]	1	L2
13	A.Simplify the Boolean expression using K-map F (A,B,C,D,)= Σm(0,2,3,7,11,13,14,15) [5M] B.Design a full adder. [5M]	2	L3
	OR		
14	Explain 8:1 Multiplexer and 4:1 Demultiplexer? [10M]	2	L2
15	Design 4-bit shift register using D flip-flops and explain its working with the help oftiming diagrams. [10M]	3	L3
	OR		

16	Discuss about universal shift register with neat diagram. [10M]	3	L2
17	Explain about four Micro-operations? [10M]	4	L2
	OR		
18	Applications of Logic Micro operations? [10M]	4	L3
19	Explain about Programmable array Logic (PAL) and Programmable Logic array (PLA)? [10M]	5	L2
	OR		
20	Explain about sequential Programmable device and types? [10M]	5	L2