R20 Regulation *Subject code: 3P3DB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech III Semester Supplementary Examinations, December 2024

DIGITAL LOGIC DESIGN

(Electronics & Communication Engineering)

Maximum Marks: 70 Date:06.12.2024 Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

	Part-A		
All the following questions carry equal marks (10X2M=20) Marks)		CO	Bloom Tx
1	Write short notes on binary number system?	1	L1
2	What is Binary code and Gray code ?	1	L1
3	Define don't cares.	2	L1
4	Simplify the Boolean function F(X,Y,Z)=∑m(3,4,6,7) using K-map.	2	L1
5	Design full adder using two half adders	3	L1
6	Difference between Static Hazards and Dynamic Hazards?	3	L1
7	What are registers?	4	L1
8	What are the drawbacks of ripple counters?	4	L1
9	Define i) state table ii) state diagram.	5	L1
10	Write Hazards types in sequential circuits.	5	L1
	Part-B		
Answer All the following questions. (5X10M=50Marks)		CO	Bloom Tx
11	A. Convert the gray number 101101into: [5M] i) Decimal ii)Octal iii)Hex B. Perform the subtraction in BCD using 9's complement method for 592.6-887.9? [5M]	1	L2
	OR		
12	A. Perform the XS- 3 subtraction in 920-356? [5M] B. Encode data bits 1010 in to the 7-bit even parity Hamming code. [5M]	1	L2
13	Minimize the following expression using K-map and realize using NAND Gates. F (A,B,C,D) = ∑m (0,1,2,9,11) +d(8,10,14,15) [10M]	2	L2
	OR		
14	Simplify the following Boolean function using Tabular method. F(A,B,C,D)=∑m(0,1,2,5,7,8,9,10,13,15) [10M]	2	L2
15	Realize the Full Subtractor using NAND gates and NOR gates? [10M]	3	L2

	OR		
16	Design 4-bit Comparator Circuit. [10M]	3	L2
17	a) Explain about serial in parallel out shift register with a neat diagram. [5M] b) Design a synchronous counter with T-flip flops that goes through the binary repeated sequence 0,1,3,7,6,4,0,1….. [5M]	4	L2
	OR		
18	a) Convert SR flip flop to JK flip flop [7M] b) What is the difference between D-latch and D-flip flop and draw the timing diagram for both. [3M]	4	L2
19	Design of a sequence detector with applications. [10M]	5	L2
	OR		
20	a) Write the steps in analyzing of sequential circuit. [5M] b) Write the procedure for synthesis of finite state machines. [5M]	5	L2