



**B.Tech IV Semester Supplementary Examinations, December 2024**

**COMPUTER ORGANIZATION  
(CSE)**

**Maximum Marks: 70**

Date:05.12.2024

Duration: 3 hours

- Note: 1.This question paper contains two parts A and B.  
 2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.  
 3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.  
 4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10X2M=20) Marks)		CO	Bloom Tx
1	Explain when an instruction is said to be complete?	1	L1
2	What are the functional units of a computer.	1	L1
3	Write the concept predecoded instruction byte queue.	2	L1
4	What is the function of 8086 index registers?	2	L1
5	What is the Fixed point representation.	3	L1
6	What is handshaking.	3	L1
7	What is a memory address map.	4	L1
8	What is the concept of polling.	4	L1
9	Mention down the three major pipeline hazards.	5	L1
10	Differentiate between ROM and PROM.	5	L1

Part-B

Answer All the following questions. (5X10M=50Marks)		CO	Bloom Tx
11	What is the difference between a direct and indirect address instruction. Explain about instruction cycle with a neat sketch. [10M]	1	L2
OR			
12	Discuss the concept of Microprogrammed control unit. [10M]	1	L2
13	A) Explain about register organization in 8086 [5M] B) Explain about the concept of segmented memory with a neat diagram. Explain it's advantages. [5M]	2	L2
OR			
14	A) Draw and discuss the read and write cycle timing diagrams of 8086 in minimum mode? [5M] B)Write about I/O address capability of 8086 [5M]	2	L2
15	Draw a flow chart for multiplication operation and explain. [10M]	3	L2
OR			
16	Explain the concept of data transfer modes. [10M]	3	L2

17	Write about the associate memory. [10M]	4	L2
	OR		
18	Explain about the cache memory and its advantages. [10M]	4	L2
19	Explain about the time shared common bus and discuss the structure for multiprocessors. [10M]	5	L2
	OR		
20	Define RISC and explain the concept of delayed load and delayed branch. [10M]	5	L2