R18 Regulation *Subject code:2P4DD*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech IV Semester Supplementary Examinations, December 2024

LINEAR & DIGITAL IC APPLICATIONS

(ECE)

Maximum Marks: 70 Date:10.12.2024 Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A			
All the following questions carry equal marks (10X2M=20) Marks)		CO	Bloom Tx
1	List features of 741 op-amp.	1	L1
2	What is Zero crossing detector?	1	L1
3	List various applications of IC 555 Timer.	2	L1
4	Define capture range and lock range.	2	L1
5	Define resolution and settling time.	3	L1
6	Mention the advantages and disadvantages of Dual slope ADC.	3	L1
7	Define noise margin and propagation delay.	4	L1
8	Define Decoder.	4	L1
9	How to convert JK flipflop to D flipflop?	5	L1
10	Define ROM and programmable logic array.	5	L1
Part-B			
Answer All the following questions. (5X10M=50Marks)		CO	Bloom Tx
11	Draw and explain the circuit diagram of instrumentation amplifier and derive the expression for gain. [10M]	1	L2
	OR		
12	A) Design a differentiator circuit that will differentiate input signal with fmax = 100Hz. [5M] B) What is a comparator? Discuss the non-inverting comparator and obtain its input and output waveforms. [5M]	1	L2
13	Explain triangular waveform generator using IC 741 and derive frequency of oscillations. [10M]	2	L2
	OR		
14	Explain square wave generator using IC 741 and derive frequency of oscillations. [10M]	2	L2
15	Draw the circuit diagram of R-2R ladder DAC and explain its operation. [10M]	3	L2
	OR		
16	Explain the principle of operation of Successive Approximation ADC. [10M]	3	L2

17	Explain about TTL driving CMOS and CMOS driving TTL with noise margin levels. [10M]	4	L2
	OR		
18	Explain with neat diagram interfacing of TTL gate driving CMOS and CMOS driving TTL Gates. [10M]	4	L2
19	Differentiate between ripple counter and synchronous counter? Design a 3- bit synchronous counter. [10M]	5	L2
	OR		
20	Draw and explain 4-bit universal shift register. [10M]	5	L2