R20 Regulation *Subject code:3O7EA*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech VII Semester Supplementary Examinations, November 2025

EMBEDDED SYSTEM DESIGN

(CSE)

Maximum Marks: 70 Date: 01.12.2025 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10X2M=20 Marks)		Marks	CO	BTL
1	Distinguish between General purpose computing systems and embedded systems?	2M	1	L1
2	Write the disadvantages of embedded system.	2M	1	L1
3	What are the languages used in embedded system?	2M	2	L1
4	Compare RISC & CISC processors?	2M	2	L1
5	What is the role of real time clock in embedded system?	2M	3	L1
6	What are the different alliances available for embedded system designs?	2M	3	L1
7	What is an Operating system? What are its Primary functions?	2M	4	L1
8	What is task control block (TCB)?	2M	4	L1
9	Define Coffman conditions?	2M	5	L1
10	How multiple threads of a process co-operate?	2M	5	L1

Part-B

Answer All the following questions. (5X10M=50Marks)		Marks	CO	BTL
11	Explain the purpose of embedded systems in detail with illustrative examples?	10M	1	L2
	OR			
12	What is the non-operational quality attribute? Explain the important non-operational quality attributes to be considered in any embedded system?	10M	1	L2
13	Explain the components of typical embedded systems in detail with neat diagram?	10M	2	L2
	OR			
14	Write short notes on Reset circuit, brown out protection circuit & watchdog timer.	10M	2	L2
15	Explain the sequence of operation for communicating with SPI bus device with neat diagram	10M	3	L2
	OR			

16	Describe the processor trends in embedded system.	10M	3	L2
17	Explain the Process life cycle in detail with neat diagram?	10M	4	L2
	OR			
18	Explain different multitasking models in the operating system context	10M	4	L2
19	Explain in detail the different task communication synchronization issues encountered in Inter Process communication?	10M	5	L2
	OR			
20	Explain the architecture of device driver, with neat sketch and give the applications of device drivers?	10M	5	L2