*R20 Regulation* *Subject code:3E8DA*

# TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

## B.Tech VIII Semester Supplementary Examinations, November 2025

## LOW POWER VLSI DESIGN

## *(ECE)*

***Maximum Marks: 70*** Date:25.11.2025 Duration: 3 hours

**Note:** **1.This question paper contains two parts A and B.**
**2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.**
**3. Part B consists of 5 Units. Answer any one full question from each unit.**
**4. Each question carries 10 marks and may have a, b, c, d as sub questions.**

Part-A

| All the following questions carry equal marks (10X2M=20 Marks) | | Marks | CO | BTL |
|---|---|---|---|---|
| 1 | Write about sources of leakage power with neat diagram. | 2M | 1 | L1 |
| 2 | Write about Drain Induced Barrier Lowering of NMOS transistor. | 2M | 1 | L1 |
| 3 | Define parallel processing. | 2M | 2 | L1 |
| 4 | What are the measures for mask level? | 2M | 2 | L1 |
| 5 | Write the drawbacks of carry look ahead adder. | 2M | 3 | L1 |
| 6 | Write the drawbacks of ripple carry adder. | 2M | 3 | L1 |
| 7 | List out the types of multiplier architectures. | 2M | 4 | L1 |
| 8 | Define binary array multiplier | 2M | 4 | L1 |
| 9 | Draw the self-refresh circuit. | 2M | 5 | L1 |
| 10 | What are the specification of ROM? | 2M | 5 | L1 |

Part-B

| Answer All the following questions. (5X10M=50Marks) | | Marks | CO | BTL |
|---|---|---|---|---|
| 11 | Explain about switching power dissipation and short circuit power dissipation. | 10M | 1 | L2 |
| | OR | | | |
| 12 | Explain about short channel effects of a transistor. | 10M | 1 | L2 |
| 13 | With a neat sketch, explain a multiple threshold CMOS inverter circuit. | 10M | 2 | L2 |
| | OR | | | |
| 14 | With a neat sketch, explain architectural level approaches? | 10M | 2 | L2 |
| 15 | Design a carry-out circuit of 4 bit carry look ahead adder. | 10M | 3 | L2 |
| | OR | | | |
| 16 | Explain the basic theory, operation & performance evaluation of carry look-ahead adders. | 10M | 3 | L2 |
| 17 | What are the building blocks are needed for binary array multiplier and explain? | 10M | 4 | L2 |
| | OR | | | |
| 18 | Construct Braun Multiplier and explain its operation. | 10M | 4 | L2 |

| | | | | |
|---|---|---|---|---|
| 19 | With a neat diagram, explain the block diagram of DRAM architecture. | 10M | 5 | L2 |
| | OR | | | |
| 20 | Discuss low power SRAM technologies with neat diagrams. | 10M | 5 | L2 |