R20 Regulation *Subject code:3P6DD*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech VI Semester Supplementary Examinations, December 2024

VLSI DESIGN
(ECE)

Maximum Marks: 70 Date:04.01.2025 Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10X2M=20) Marks)		CO	Bloom Tx
1	Define body effect.	1	L1
2	Define figure of merit.	1	L1
3	List different MOS layers.	2	L1
4	What is stick diagram?	2	L1
5	List the sources of wiring capacitance.	3	L1
6	Define Switch logic.	3	L1
7	What are different types of Serial Access Memories	4	L1
8	Draw the circuit diagram of full adder.	4	L1
9	What are programmable logic devices?	5	L1
10	Define Stuck open faults.	5	L1

Part-B

Answer All the following questions. (5X10M=50Marks)		CO	Bloom Tx
11	Use neat sketches and explain n-MOS fabrication process. [10M]	1	L4
	OR		
12	Illustrate the operation of NMOS enhancement transistor in detail. [10M]	1	L3
13	Use flow chart of VLSI Design flow and explain the operation of each step-in detail. [10M]	2	L3
	OR		
14	Draw the CMOS logic circuit, stick diagram and layout for the following Boolean expression F = [A.(B+C)]. [10M]	2	L4
15	Explain in detail about Dynamic CMOS logic and CMOS Domino logic gates with suitable example. [10M]	3	L4
	OR		
16	Describe three sources of wiring capacitance. [10M]	3	L3
17	A) Draw the logic diagram of zero/one detector and explain its operation. [5M] B) Explain about ALU subsystem. [5M]	4	L4 L3

	OR			
18	Draw and explain the operation of SRAM cell.	[10M]	4	L4
19	Explain the architecture of FPGA with neat diagram.	[10M]	5	L4
	OR			
20	Discuss chip level testing techniques.	[10M]	5	L3