R20 Regulation *Subject code:3E5DA*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech V Semester Supplementary Examinations, December 2024

DIGITAL DESIGN THROUGH VERILOG HDL

(ECE)

Maximum Marks: 70 Date:08.01.2025 Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

	Part-A		
All the following questions carry equal marks (10X2M=20) Marks)		CO	Bloom Tx
1	Explain simulation and synthesis with differences	1	L1
2	Mention data types used in Verilog HDL	1	L1
3	Illustrate with an example Array of Instances of Primitives	2	L1
4	Define net delay with an example	2	L1
5	Define gate delays with example.	3	L1
6	Write about Arithmetic operators in Verilog.	3	L1
7	Explain continuous assignment statements.	4	L1
8	Difference between inter and intra assignment delay	4	L1
9	Write about UDP's	5	L1
10	Write difference between task and functions	5	L1
	Part-B		
Answer All the following questions. (5X10M=50Marks)		CO	Bloom Tx
11	A) Explain levels of design description. [5M] B) Differentiate between vectors and memories. [5M]	1	L2
	OR		
12	A) Explain the following "lexical conventions" with examples. [5M] (i) key words (ii) identifiers (iii) Numbers B) Explain about data types in Verilog. [5M]	1	L2
13	A) Design full subtractor using basic logic primitives. [5M] B) Write the Verilog code for 3x8 decoder using gate level modeling. [5M]	2	L2
	OR		
14	A) Classify strengths in Verilog with appropriate examples. [5M] B) Write a Verilog code for 2 input nand gate and its test bench code. [5M]	2	L2
15	A)Write Verilog module for BCD adder using dataflow modeling? [5M] B)Design module and test bench for clocked SR-flip-flop. [5M]	3	L2

	OR		
16	A)Discuss the basic transistor switches? What is the difference between basic and resistive MOS switches. [5M] B)Develop switch level program for CMOS NAND gate. [5M]	3	L2
17	A) Compare and contrast Begin-End and Fork-Join blocks with example. [5M] B) Compare and contrast between tasks and functions. [5M]	4	L2
	OR		
18	A) Design 4:1 multiplexer in behavioral modeling style. [5M] B) Explain disable construct with example. [5M]	4	L2
19	A) Explain about parameter with Verilog code. [5M] B) Explain about compiler directives. [5M]	5	L2
	OR		
20	Explain about path delays with example [10M]	5	L2