Regulation R17 *Subject code:1E5DE*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech III Year I Semester Supplementary Examinations, December 2024

DIGITAL DESIGN THROUGH VERILOG HDL

(ECE)

Maximum Marks: 70 Date:06.01.2025 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks **(10x2M=20 Marks)**

Q.NO	QUESTIONS	CO	Blooms Tx
1	Explain simulation and synthesis with differences	CO1	L2
2	Mention data types used in Verilog HDL	CO1	L1
3	Illustrate with an example Array of Instances of Primitives	CO2	L1
4	Define gate delays with example.	CO2	L1
5	Write about Arithmetic operators in Verilog.	CO3	L2
6	Explain continuous assignment statements.	CO3	L1
7	What are parallel blocks?	CO4	L1
8	Difference between inter and intra assignment delay	CO4	L2
9	Define task with an example	CO5	L1
10	Write a syntax for $monitor	CO5	L1

Part-B

Answer All the following questions. **(10M X 5=50Marks)**

11	a) Explain levels of design description. [5M]	CO1	L3
	b) Differentiate between vectors and memories. [5M]	CO1	L4
	OR		
12	a) Explain the following "lexical conventions" with examples. [5M] (i) key words (ii) identifiers (iii) Numbers	CO1	L4
	b)Explain about data types in Verilog. [5M]	CO1	L4
13	a) Design full subtractor using basic logic primitives. [5M]	CO2	L3
	b) Write the Verilog code for 3x8 decoder using gate level modeling. [5M]	CO2	L3
	OR		
14	a) Classify strengths in Verilog with appropriate examples. [5M]	CO2	L4
	b) Write a Verilog code for 2 input NAND gate and its test bench code. [5M]	CO2	L4

15	a) Write the Verilog code for 4-bit ALU also obtain its test bench and simulation results using conditional operator[5M]	CO3	L2
	b) Design CMOS switch with a single control line. [5M]	CO3	L3
	OR		
16	a) Design 4 to 1 multiplexer in data flow modeling with test bench and results[5M]	CO3	L3
	b) Develop switch level program for CMOS NOR gate[5M]	CO3	L2
17	a) Explain about procedural assignment statements usage in Verilog. [5M]		
	b) Design 3-bit counter module and test bench using behavioral modeling. [5M]	CO4	L4
	OR		
18	a) Design 4:1 multiplexer in behavioral modeling style. [5M]	CO4	L4
	b) Explain disable construct with example. [5M]	CO4	L4
19	a) Explain $strobe task with an example [5M]	CO5	L4
	b) Explain about compiler directives [5M]	CO5	L3
	OR		
20	a) Explain about file based tasks [5M]	CO5	L3
	b) Design a Moore machine (FSM) with an example [5M]		