R22 Regulation *Subject code: 4E4BB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech IV Semester Regular Examinations, July 2024

DIGITAL ELECTRONICS

(EEE)

Maximum Marks: 60 Date:20.07.2024 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 10 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

	Part-A	CO	Bloom Tx
All the following questions carry equal marks	(10X1M=10 Marks)		
1.a)	The number $(1333)_6$ converts into base 10	1	L3
b)	Define switching algebra and complementation	1	L2
c)	Obtain the PI, EPI for given function f(A, B, C)=∑(0,3,5,7)	2	L3
d)	Draw a logic diagram of EXOR gate and NAND gate	2	L2
e)	Compare between combination circuit and sequential circuits	3	L3
f)	How many 2X1 MUX required to implementation of 16 X1 MUX	3	L3
g)	Explain the T flip flop Truth table	4	L2
h)	Define shift register.	4	L2
i)	Define State Diagram.	5	L1
j)	Define Merger graph.	5	L1
	Part-B		
Answer All the following questions.	(5X10M=50Marks)		Bloom Tx level
2	Convert the following numbers in the way specified: [10M] i. $(11001011.1001)_2$ to base 10 ii. $(83.375)_{10}$ to base 2 iii. $01101001.0111)_2$ to base 16 iv. $(11010101)_2$ to Gray code	1	L3
	OR		
3	A. Determine the canonical sum-of-products representation of the functions $f(x, y, z) = x + (x'y' + x'z)'$ B. State and prove De Morgan's laws. [5+5]	1	L3 L3
4	Minimization the switching functions $f(w, x, y, z) = \sum m(1, 3, 4, 5, 9, 10, 11) + \sum d(6, 8)$ and draw a logic circuit diagram in universal logic. [10]	2	L3
	OR		
5	A. Determine the minimal sum-of-products expression for $f(w, x, y, z) = \sum(0, 2, 4, 9, 12, 15) + \sum_{\varphi}(1, 5, 7, 10)$	2	L3

	B. Simplify the function using the tabular method f1 (v, w, x, y, z)= ∑(3, 6, 7, 8, 10, 12, 14, 17, 19, 20, 21, 24, 25, 27, 28) [5+5]		L3
6	A. Implement the function using MUX for F (w, x, y, z) = ∑(0, 1, 4, 5, 6, 7, 9, 11, 15) B. Design Combinational circuit for 4 bit binary to gray code converter. [5+5]	3	L3 L3
	OR		
7	A. Design a Full Adder and draw a circuit diagram using NOR gates. B. Design the 3-bit magnitude comparator. [5+5]	3	L3 L3
8	What are the disadvantages of JK Flip Flop, draw and explain JK flip flop logic diagram, characteristic equation and excitation table. [10]	4	L3
	OR		
9	A. Design a mod 5 ripple counter. B. Design a 4 bit ring Counter. [5+5]	4	L3 L3
10	A. Write the capabilities and limitations of FSM? B. Minimize the no. of staes in a given below completley specified machine using partition technique. [5+5]	5	L2 L4
	OR		
11	A. Differences between mealy and moore machines? B. Obtain maximum compatibility for the following state table using merger chart and merge table. [5+5]	5	L2 L4

P.S	N.S. O/P	
	X=0	X=1
A	B,0	E,0
B	E,0	D,0
C	D,1	A,0
D	B,1	E,0
E	C,0	D,0

PS	NS, Z			
	00	01	11	10
A	--	C,-	--	-,1
B	A,1	--	B,0	--
C	--	--	--	D,1
D	C,-	A,-	C,-	F,0
E	B,-	B,-	A,-	-,0
F	-.0	C,1	--	H,1
G	-,1	E,1	--	D,1
H	-,1	G,-	--	F,1