R22 Regulation *Subject code: 4E3FB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech III Semester Supplementary Examinations, July 2024

COMPUTER ORGANIZATION AND ARCHITECTURE

(IT)

Maximum Marks: 60 Date:27.07.2024 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 10 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

	Part-A	CO	Bloom Tx
All the following questions carry equal marks (10x1M=10 Marks)			
1.a)	Define Micro-Operation.	CO1	L1
b)	Define Interrupt Cycle.	CO1	L1
c)	List the steps to fetch an Instruction.	CO2	L1
d)	What is the primary function of a hardwired control unit?	CO2	L1
e)	What are the 5 stages of pipelining?	CO3	L1
f)	What is the purpose of a pipeline register?	CO3	L1
g)	Define Cache memory.	CO4	L1
h)	Why are the Read and Write Control lines in a DMA Controller Bidirectional?	CO4	L1
i)	Define SATA.	CO5	L1
j)	Explain about I/O Module.	CO5	L1
	Part-B		
Answer All the following questions. (5X10M=50Marks)			Bloom Tx level
2	Explain the various modes of addressing with numerical example. [10M]	CO1	L3
	OR		
3	Explain the role of hardware circuits, such as multipliers, in performing unsigned multiplication. [10M]	CO1	L3
4	A. What are the steps involved in an instruction cycle? [5M] B. How do control signals facilitate communication between different components of a computer system? [5M]	CO2	L1
	OR		
5	How does the Basic Processing Unit handle arithmetic and logic operations in computing tasks? [10M]	CO2	L3
6	Explain the concept and significance of multiple internal buses in computer architecture, highlighting their role in facilitating efficient communication among different components within a system. [10M]	CO3	L3

	OR		
7	Explain the concept of throughput and latency in the context of pipelining performance evaluation. [10M]	CO3	L3
8	Draw the block diagram of DMA Controller and DMA Transfer of data with relevant information. [10M]	CO4	L2
	OR		
9	Write a short note on i) RAM [3M] ii) ROM [3M] iii) Hit Ratio [4M]	CO4	L1
10	A. How does arbitration play a role in managing resource access conflicts? [5M] B. What role do interrupt service routines (ISRs) play in managing program-controlled I/O operations? [5M]	CO5	L1
	OR		
11	Illustrate the role of I/O organization in enhancing the overall functionality and responsiveness of computer systems. [10M]	CO5	L2