R22 Regulation *Subject code: 4E3ED*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech III Semester Supplementary Examinations, July 2024

COMPUTER ARCHITECTURE AND ORGANIZATION

(Common to CSE & CSE(AI&ML))

Maximum Marks: 60 Date:27.07.2024 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 10 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

	Part-A	CO	Bloom Tx
All the following questions carry equal marks (10X1M=10 Marks)			
1.a)	List two important instruction set design issues?	1	L1
b)	What operations are included in micro-operations?	1	L1
c)	What is the need of having many addressing modes in machine ?	2	L1
d)	Define the necessary factors for instruction sequencing.	2	L1
e)	When exponent overflow and underflow occur?	3	L1
f)	How subtraction operation and other operations can be simplified in a digital system?	3	L1
g)	List two peripherals devices that produce an acceptable output for a person to understand.	4	L1
h)	What is the purpose of I/O interface?	4	L1
i)	What is the role of cache in pipelining?	5	L1
j)	List two characteristics of Multi processors.	5	L1
	Part-B		
Answer All the following questions. (5X10M=50Marks)			Bloom Tx level
2	a) List and explain the functional units of a computer. [5] b) Explain in detail about common bus system. [5]	1	L1,L2
	OR		
3	a) Explain the different methods used for handling the situation when multiple interrupts occurs. [5] b) How many references to memory are needed for each type of instruction to bring an operand into a processor register? Explain. [5]	1	L2 L2
4	a) Discuss the Physical memory organization. [5] b) Give a brief note on instruction cycle. [5]	2	L6 L2
	OR		
5	a) Explain the register organization in 8086. [5] b) List the advantages and disadvantages of hardwired control over micro-programmed control. [5]	2	L2 L1

6	Describe Explain about booth multiplication with example. [10]	3	L2
	OR		
7	a) Explain the flowchart for floating point subtraction with neat diagram. [5] b) Explain in detail about division algorithm. [5]	3	L2 L2
8	a) Describe virtual-memory address-translation method based on the concept of fixed-length pages with a neat block diagram. [5] b) Summarize and list out memory hierarchy according to the speed and size. [5]	4	L3 L2
	OR		
9	Explain about the DMA controller with a block diagram. [10]	4	L2
10	a) What is instruction pipelining? What are the conflicts that occurred during instruction pipelining? [5] b) Give the major characteristics of RISC and CISC architectures. [5]	5	L1
	OR		
11	a) Explain inter processor communication and synchronization in a shared multiprocessor environment. [5] b) What are the various forms available for establishing an interconnection network in a multi processor system? [5]	5	L2 L1