R20 Regulation *Subject code: 3P4EB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech IV Semester Supplementary Examinations, July 2024

COMPUTER ORGANIZATION AND ARCHITECTURE

(CSE)

Maximum Marks: 70 Date:20.07.2024 Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

	Part-A		
All the following questions carry equal marks (10X2M=20 Marks)		CO	Bloom Tx
1	Define the term Computer Architecture.	1	L1
2	What is an instruction cycle.	1	L1
3	What is the difference between Near and Far Procedure?	2	L1
4	What is meant by instruction?	2	L1
5	Briefly explain the following representations: sign magnitude	3	L1
6	Write any 2 problems with signed binary integer representation	3	L1
7	Define Hit and Miss with respect to Cache memory	4	L1
8	Define asynchronous bus	4	L1
9	How the timeslice method works	5	L1
10	What is a Semaphore	5	L1
	Part-B		
Answer All the following questions. (5X10M=50Marks)			
11	Write in detail about Memory Reference Instructions and Register Reference instructions. [10]	1	L2
	OR		
12	A. Explain about Input-output and Interrupt. [5] B. Write in detail bout Computer Instructions. [5]	1	L2
13	A. Explain Timing and control with Timing diagram. [5] B. Describe any six Addressing modes of 8086 with suitable example. [5]	2	L2
	OR		
14	A. Draw the Microprocessor architecture and identify all the parts. [5] B. Explain maximum mode execution of 8086 microprocessor. [5]	2	L2
15	A. Write about Arithmetic and Logic Unit with neat diagram. [5] B. Explain Integer representation. [5]	3	L2
	OR		
16	A. IEEE Standard for Binary Floating-Point Representation. [5]	3	L2

	B. Explain Floating point arithmetic for Addition and Subtraction. [5]		
17	Discuss the various mapping techniques used in cache memories. [10]	4	L2
	OR		
18	A. Draw the neat sketch of memory hierarchy and explain the need of cache memory? [5] B. Explain about direct and set associative map technique in cache. [5]	4	L2
19	A, Explain how Flynn classified the processors into different streams by giving an example for each stream. [5] B. Explain tightly coupled and loosely coupled systems with suitable examples. [5]	5	L2
	OR		
20	A. Explain serial arbitration (Daisy Chain). [5] B. Explain parallel arbitration. [5]	5	L2