R20 Regulation *Subject code:3P4BB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech IV Semester Supplementary Examinations, July 2024

Digital Electronics

(EEE)

Maximum Marks: 70 Date:20.07.2024 Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10X2M=20 Marks)		CO	Bloom Tx
1	Write short notes on binary number system?	1	L2
2	Convert binary value 1011010 to gray value?	1	L2
3	Explain About the Basic gates?	2	L3
4	Write short notes on Universal gates?	2	L1
5	Write about 2X1 MUX.	3	L3
6	Difference between Static Hazards and Dynamic Hazards?	3	L3
7	What are registers? Write any two applications.	4	L2
8	Difference between a latch and a flip-flop.	4	L3
9	List the capabilities of finite state machine.	5	L1
10	What is a state diagram?	5	L3
	Part-B		
Answer All the following questions. (5X10M=50Marks)			
11	a) Encode the message bits $(1110)_2$ into 7-bit even parity hamming code. (7M) b) Given that $(81)_{10} = (100)_b$, Find the value of b. (3M)	1	L4 L3
	OR		
12	a) Convert $(736)_{10} = (\ )_2$, $(\ )_8$, $(\ )_{16}$ (6M) b) Add the BCD addition of 204.6+185.5 (4M)	1	L3
13	Minimize the following expression using K-map and realize using NAND Gates. $F(A,B,C,D) = \sum m(0,1,2,9,11) + d(8,10,14,15)$. (10M)	2	L3
	OR		
14	Simplify the following Boolean function using Tabular method. $F(A,B,C,D) = \sum m(0,1,2,5,7,8,9,10,13,15)$ (10M)	2	L3
15	Realize the Full Subtractor using NAND gates and NOR gates? (10M)	3	L3
	OR		

16	Design 4-bit Comparator Circuit. (10M)	3	L2
17	Design a mod-12 Ripple counter using T flip flops and explain its operation. (10M)	4	L2
	OR		
18	a). What do you mean by universal shift register? Draw and explain its circuit diagram and operation. (4M) b). Design a MOD-10 ripple counter. (6M)	4	L3
19	Design Mealy circuit to detect the sequence 1 1 0 1. (10M)	5	L3
	OR		
20	Draw the diagram of Mealy type FSM and explain with an example. (10M)	5	L3