R20 Regulation *Subject code:3P3EC*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech III Semester Supplementary Examinations, July 2024

LOGIC CIRCUITS DESIGN

(Common to CSE & CSE(AI&ML))

Maximum Marks: 70 Date:23.07.2024 Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

	Part-A		
All the following questions carry equal marks (10X2M=20 Marks)		CO	Bloom Tx
1	State De Morgan's theorem.	1	L1
2	Convert decimal 153 to octal.	1	L1
3	What is a K- map? Draw the diagram of 4 variable K-map?	2	L1
4	Define sequential logic circuit.	2	L1
5	Define shift register.	3	L1
6	What are the Micro operations?	3	L1
7	List the arithmetic micro-operations and logic micro-operations.	4	L1
8	Discuss about three state bus buffers.	4	L1
9	Differentiate RAM with ROM.	5	L1
10	Write about programmable logic array ?	5	L1
	Part-B		
Answer All the following questions. (5X10M=50Marks)			
11	(a)Explain in short about the axiomatic definition used in Boolean algebra. [5M] (b) Prove that ABC + ABC' + AB'C + A'BC = AB + AC + BC [5M]	1	L2
	OR		
12	(a) Explain in detail about universal gates with neat diagram. [5M] (b) Express the Boolean function F=A+B'C as a sum of minterms. [5M]	1	L2
13	(a) Simplify the Boolean expression using K-map [5M] F (A,B,C,D)= Σ (0,1,2,4,5,6,8,9,12,13,14) (b) Design a full adder. [5M]	2	L2
	OR		
14	(a)Explain about 8:1 Multiplexer with neat diagram. [6M] (b)Design decimal adder. [4M]	2	L2
15	(a) What is shift register? Explain different modes of operation of Shift Registers? [5M]	3	L2

	(b) Explain synchronous and ripple counters compare their merits and demerits? [5M]		
	OR		
16	(a) Discuss about universal shift register with neat diagram. [5M] (b)With a neat diagram explain in detail about master slave edge triggered D Flip-Flop. [5M]	3	L3
17	(a) With a neat diagram explain in detail about Arithmetic Logic Shift Unit. [5M] (b) What is control function and also explain with its hardware implementation? [5M]	4	L2
	OR		
18	With a neat diagram construct a bus system for 4 registers using multiplexers and also using tri state buffers. [10M]	4	L3
19	Discuss in detail about PLA &PAL. [10M]	5	L2
	OR		
20	What is memory decoding? Explain about the construction of 4 X 4 RAM? [10M]	5	L2