R20 Regulation *Subject code: 3P3DB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech III Semester Supplementary Examinations, July 2024

DIGITAL LOGIC DESIGN

(ECE)

Maximum Marks: 70 Date:23.07.2024 Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

	Part-A		
All the following questions carry equal marks (10X2M=20 Marks)		CO	Bloom Tx
1	Write short notes on binary number system?	1	L2
2	What is Binary code and Gray code?	1	L2
3	State and Prove Demorgan's theorem.	2	L2
4	Simplify the Boolean function $F(X,Y,Z)=\sum m(3,4,6,7)$ using K-map.	2	L2
5	Design 2x4 decoder using AND gates.	3	L2
6	What is a decoder? Write its applications.	3	L2
7	What are registers? Write any two applications.	4	L2
8	Difference between a latch and a flip-flop.	4	L2
9	List the capabilities of finite state machine.	5	L1
10	Write Hazards types in sequential circuits.	5	L3
	Part-B		
Answer All the following questions. (5X10M=50Marks)			
11	a) Convert the given Gray code number to equivalent binary 01001011110010. (5M) b) Convert $(A0F9.0DC)_{16}$ to decimal, binary, octal. (5M)	1	L2
	OR		
12	a) Subtract 745.81-436.62 using the 9's Compliment method? (5M) b) Perform the XS-3 addition in 37+28. (5M)	1	L3
13	Simplify the following expression using tabulation method $y(w,x,y,z)=\sum m(1,2,3,5,6,7,8,9,12,13,15)$ (10M)	2	L3
	OR		
14	a).Minimize the following expression using K-map and realize using NOR Gates. $f=\sum m(0,4,6,7,8,12,13,14,15)$. (6M) b) Prove that AB'C + B + BD'+ ABD'+ A'C = B +C. (4M)	2	L4
15	Realize the Full Subtractor using NAND gates and NOR gates? (10M)	3	L2

	OR		
16	a) Design a 4-bit even parity generator and checker? (5M) b) Design a 4-bit binary-to – BCD code converter? (5M)	3	L4
17	a) Explain about serial in parallel out shift register with a neat diagram. (5M) b) Design a synchronous counter with T-flip flops that goes through the binary repeated sequence 0,1,3,7,6,4,0,1….. (5M)	4	L3
	OR		
18	a) Convert SR flip flop to JK flip flop (5M) b) What is the difference between D-latch and D-flip flop and draw the timing diagram for both. (5M)	4	L3
19	Design of a sequence detector with applications. (10M)	5	L3
	OR		
20	Draw the diagram of Mealy type FSM and explain with an example. (10M)	5	L3