R18 Regulation *Subject code: 2P4DD*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech IV Semester Supplementary Examinations, July 2024

LINEAR & DIGITAL IC APPLICATIONS

(ECE)

Maximum Marks: 70 Date:25.07.2024 Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

	Part-A		
All the following questions carry equal marks (10X2M=20 Marks)		CO	Bloom Tx
1	List features of 741 op-amp.	1	L1
2	What is Zero crossing detector?	1	L1
3	Classify different types of filters.	2	L1
4	List the features of IC 555.	2	L1
5	Define resolution and settling time.	3	L1
6	Mention the advantages and disadvantages of Dual slope ADC.	3	L1
7	Write a short note on priority encoder.	4	L1
8	Sketch the 4x16 decoder using 74LS138 IC's.	4	L1
9	Write the Truth table of JK flip flop	5	L1
10	Classify types of ROMs.	5	L1
	Part-B		
Answer All the following questions. (5X10M=50Marks)			
11	Draw the circuit diagram of a two input non-inverting summing amplifier and derive the expression for the output voltage. [10M]	1	L2
	OR		
12	a) Design a differentiator circuit that will differentiate input signal with fmax = 100Hz. [5M] b) What is a comparator? Discuss the non inverting comparator and obtain its input and output waveforms. [5M]	1	L2
13	Derive the expression for the transfer function of first order low pass filter with a neat diagram. [10M]	2	L2
	OR		
14	a) Draw the block diagram of Astable multivibrator using 555timer and derive an expression for its frequency of oscillations. [5M] b) A 555 timer Astable multi vibrator uses RA = 6.8 kΩ, RB = 3.3 kΩ and C = 0.1 μf. Calculate the free running frequency of oscillations. [5M]	2	L2

15	a) Draw the circuit diagram of Inverted R-2R ladder DAC network. Explain its working. [5M] b) Calculate analog output voltage in Inverted R-2R DAC if V_{ref}=12v and input digital word is 101010. [5M]	3	L2
	OR		
16	Explain the principle of operation of Successive Approximation ADC. [10M]	3	L2
17	Design a 5 to 32line decoder using 3 to 8line decoder, active low outputs with 2 active low and one active high enable. [10M]	4	L2
	OR		
18	a) Compare various logic families. [5M] b) Implement the following Boolean expression using 74×151 IC F(z)=AB+BC+AC. [5M]	4	L3 L2
19	Differentiate between ripple counter and synchronous counter? Design a 3- bit synchronous counter. [10M]	5	L4
	OR		
20	a) Draw and explain 4-bit universal shift register. [5M] b) Design a Modulo-12 ripple counter using 74×74. [5M]	5	L2 L2