



**B.Tech IV Semester Supplementary Examinations, July 2024**

**DIGITAL LOGIC DESIGN  
(EEE)**

**Maximum Marks: 70**

Date: 25.07.2024 Duration: 3 hours

- Note:
1. This question paper contains two parts A and B.
  2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
  3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
  4. Each question carries 10 marks and may have a, b, c, d as sub questions.

**Part-A**

All the following questions carry equal marks		(10X2M=20 Marks)	CO	Bloom Tx
1	What is Gray code?		1	L1
2	How do you obtain dual of an expression?		1	L1
3	What are don't cares?		2	L1
4	Define the full subtractor.		2	L1
5	Compare latch and flip flop.		3	L1
6	List the applications of Multiplexers		3	L1
7	Differentiate between RAM and ROM.		4	L1
8	Define the ring counter.		4	L1
9	What are finite state machines?		5	L1
10	Define sequential machine.		5	L1

**Part-B**

Answer All the following questions.		(5X10M=50Marks)		
11	a) Convert the gray number 101101 into decimal, hex, octal [5M] b) Perform the subtraction in BCD using 9's complement method for 592.6-887.9 [5M]		1	L2
OR				
12	Expand $(A+D')(A+C')(A'+B)(A'+B+C)$ into max terms and min terms. [10M]		1	L2
13	Reduce the expression using k map $F(A, B, C, D) = \sum m(0, 1, 2, 3, 5, 7, 8, 9, 10, 12, 13)$ and implement the real minimal expression in universal logic. [10M]		2	L2
OR				
14	a) Draw the circuit diagram of a full subtractor using NOR gates. [5M] b) What is decoder? Construct a 4:16 decoder with two 3:8 decoders. [5M]		2	L2
15	a) Design 4-bit shift register using D flip-flops and explain its working with the help of timing diagrams. [5M] b) Design a counter with the following repeated binary sequence: 0,1,2,3,4,5,6.....use JK flip-flops. [5M]		3	L3

	OR		
16	What is meant by Edge triggered? Differentiate SR-FF and JK-FF with their functional operation and excitation tables. [10M]	3	L3
17	Design a synchronous 3-bit Up-down counter using JK FFs. [10M]	4	L3
	OR		
18	a) Explain about Ring counter and Twisted Ring counter. [3M] b) Design a combinational circuit accepts a 3-bit binary number and generates its equivalent XS-3 code using a PROM. [7M]	4	L3
19	Explain about sequential circuits, state table and state diagram. [10M]	5	L2
	OR		
20	Explain about Mealy machine with circuit diagram. [10M]	5	L2