



B.Tech III Semester Supplementary Examinations, July 2024

**Digital Logic Design
 (Common to CSE & IT)**

Maximum Marks: 70

Date:23.07.2024 Duration: 3 hours

- Note: 1.This question paper contains two parts A and B.
 2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
 3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
 4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10X2M=20 Marks)		CO	Bloom Tx
1	Define the term digital.	1	L1
2	Draw the logic diagram and truth table for AND gate	1	L1
3	What are called don't care conditions?	2	L1
4	Define 2:1 multiplexer.	2	L1
5	Draw the block diagram of Sequential circuit?	3	L1
6	What is a latch?	3	L1
7	What is assembly level programming?	4	L1
8	What are the functional parts of 8086 CPU?	4	L1
9	Define RAM.	5	L1
10	Define memory & it's types.	5	L1

Part-B

Answer All the following questions. (5X10M=50Marks)			
11	Prove that the sum of all minterms of Boolean function for three variable is 1. [10M]	1	L2
OR			
12	Show that the dual of the Ex-or is equal to its complement? [10M]	1	L2
13	Write Short notes on [10M] a) Half adder b) Full adder c) Half subtractor d) Full subtractor	2	L2
OR			
14	Design the combinational circuit for binary to gray code conversion. [10M]	2	L2
15	Write the differences between the following. a) Combinational circuits and sequential circuit. [5M] b) Flip- flops and Latches. [5M]	3	L2
OR			

16	Write the different kinds of flip-flops. Explain the Logic diagram of SR flip-flop? [10M]	3	L2
17	Write program subtraction of TWO 16 bit no. [10M]	4	L2
OR			
18	List out the assembler directives and explain in detail. [10M]	4	L2
19	Explain about Programmable array Logic (PAL) and Programmable Logic array (PLA)? [10M]	5	L2
OR			
20	Implement the following function using PLA $F1(A,B,C) = \sum(0,1,2,4)$ $F2(A,B,C) = \sum(0,5,6,7)$ [10M]	5	L2