R18 Regulation *Subject code: 2P3DE*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech III Semester Supplementary Examinations, July 2024

PULSE AND DIGITAL CIRCUITS
(ECE)

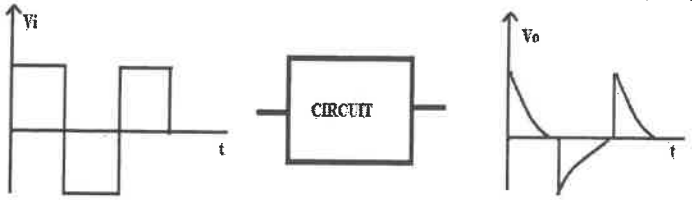
Maximum Marks: 70 Date:27.07.2024 Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10X2M=20 Marks)		CO	Bloom Tx
1	Draw the low pass RC circuit and explain its working.	1	L2
2	Write the condition of RC circuit to work as differentiator.	1	L1
3	State clamping circuit theorem.	2	L1
4	What do you mean by a regenerative comparator? Give an example.	2	L2
5	Define a diode forward recovery time and reverse recovery time	3	L1
6	Give the expression for fall time of transistor switch.	3	L2
7	Define Multivibrator.	4	L1
8	Define UTP and LTP of a Schmitt trigger.	4	L1
9	Write the principle of sampling gates.	5	L2
10	Define Positive and Negative logic systems.	5	L1

Part-B

Answer All the following questions. (5X10M=50Marks)			
11	a) Which linear circuit is required to obtain the output for the given input shown in figure? Explain its operation with necessary equations. [5M]  b) Derive the expression for rise time of the output of a low pass circuit excited by a step input and obtain relation between rise time and bandwidth. [5M]	1	L3
	OR		
12	a) Prove that for any periodic input waveform, the average level of the steady state output signal from RC high pass circuit is always zero. [5M] b) A 1 KHz symmetrical square wave of ±10V is applied to an RC circuit having 1msec time constant. Calculate and plot the output of RC High pass circuit and RC Low pass circuit. [5M]	1	L4

13	a)Draw the circuit diagram and explain the working of transistor clippers.[5M] b) Draw the basic circuit diagram of negative peak clamper circuit and explain its operation. [5M]	2	L3
	OR		
14	a)What do you mean by biased clamping? [5M] b) A 100V peak square wave with an average value of 0V and a period of 20ms is to be negatively clamped at 25V. Draw the input and output waveforms and necessary circuit diagram. [5M]	2	L4
15	a)Explain the transistor switching times. [5M] b)Draw and Explain the piece-wise linear characteristics of a diode. [5M]	3	L3
	OR		
16	Draw the circuit diagram of Transistor Bootstrap Time Base Generator and explain its operation in detail. [10M]	3	L3
17	a)What is Hysteresis and explain the different methods for avoiding Hysteresis in Schmitt trigger in detail. [5M] b) Design a Schmitt trigger circuit to have UTP=6V and LTP=3V using silicon Transistor Whose $h_{fe}(min)$=40. Assume necessary data [5M]	4	L2
	OR		
18	a)With the help of neat circuit diagram and waveform, explain the principle of operation of collector coupled Monostable Multivibrator. [5M] b) Explain how the deviation from linearity is expressed in terms of errors. [5M]	4	L3
19	a)Describe the working of a 4-Diode sampling gate with necessary diagram & equations. [5M] b) Explain the working of bi-directional gate using transistors. [5M]	5	L3
	OR		
20	Draw the circuit diagram of a positive 3 i/p NAND gate in DTL logic and explain its working. [10M]	5	L3