R18 Regulation *Subject code: 2P3DB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech III Semester Supplementary Examinations, July 2024

DIGITAL LOGIC DESIGN

(ECE)

Maximum Marks: 70 Date:20.07.2024 Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

	Part-A		
All the following questions carry equal marks (10X2M=20 Marks)		CO	Bloom Tx
1	What is Gray code?	1	L1
2	How do you obtain dual of an expression?	1	L1
3	What are don't cares?	2	L1
4	What is minterm?	2	L1
5	Compare latch and flip flop.	3	L1
6	List the applications of Multiplexers	3	L1
7	What are applications of Flip-Flop?	4	L1
8	What are the basic types of shift registers?	4	L1
9	What are drawbacks of ripple counters?	5	L1
10	Compare Mealy and Moore machines.	5	L1
	Part-B		
Answer All the following questions. (5X10M=50Marks)			
11	a). Convert the gray number 101101 into decimal, hex, octal [5M] b). Perform the subtraction in BCD using 9's complement method for 592.6-887.9 [5M]	1	L2
	OR		
12	Derive the Boolean expression for a two input Ex-OR gate to realize with the two input NAND gates without using complemented variables and draw the circuit. [10M]	1	L2
13	Simplify the expression F(A,B,C,D)=A$\bar{B}$+AB$\bar{D}$+ABD+$\bar{A}\bar{C}\bar{D}$+$\bar{A}$B$\bar{C}$ and implement with NAND gates only. [10M]	2	L2
	OR		
14	Reduce the expression using k map F(A, B, C, D) =Σm(0,1, 2, 3, 5,7,8,9,10,12,13) and implement the real minimal expression in universal logic. [10M]	2	L2

15	a) Realize 16-input multiplexer by cascading of two 8-input multiplexers. [5M] b) Realize the function f(A,B,C,D)=πM(1,4,6,10,14)+d(0,8,11,15) using: i) 16:1 MUX ii) 8:1 MUX. [5M]	3	L2
	OR		
16	Design a Full adder using Decoder. [10M]	3	L2
17	a). Draw the logic diagram of a SR latch using NOR gates. Explain its operation using excitation table. [5M] b) Convert D flip-flop into T and JK flip-flops. [5M]	4	L2
	OR		
18	What is meant by 'edge triggered'? Differentiate SR-FF and JK-FF with their functional operation and excitation tables. [10M]	4	L2
19	Explain about sequential circuits, state table and state diagram. [10M]	5	L2
	OR		
20	Explain about Mealy machine with circuit diagram. [10M]	5	L2